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SCAN CONVERTER AND REFRESH MEMORY WITH REMOTE TERMINAL AND DISP--ETC(U)

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**SCAN CONVERTER AND REFRESH MEMORY WITH REMOTE  
TERMINAL AND DISPLAY DATA INTERFACE**

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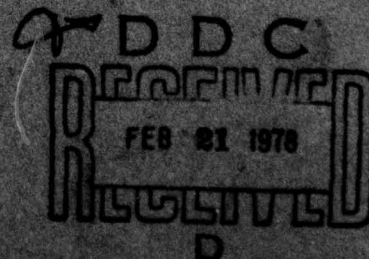
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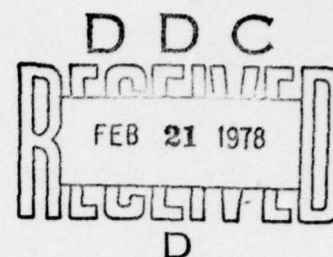
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## SECTION 1. INTRODUCTION

This equipment converts the polar-coordinate outputs of a weather radar and signal processor to cartesian-coordinate form, contours the video, then stores the resulting data in any of four independent image-oriented memories, each of which refreshes one raster-scan color television monitor.

The most significant advantage of this system over conventional monochrome radar-image-storage devices lies in the ability of the operator to unambiguously recognize sixteen color-coded levels. Stored images of PPI, RHI or THI (Time-Height) radar scans can be retained indefinitely, updated, or erased independently of each other. Front-panel controls determine distance and time scaling, origin location, range, altitude, and time marker spacing and range cell width. Contour threshold colors-- 0 (black) through 15 (red)-- and levels (0 through 99) having been set up on an array of thumbwheel switches can be entered into any or all of the displays in the form of a legend or color key.

Memory requirements have been limited to about 328,000 bits per display by performing operations such as coordinate conversion, scaling, translation, introduction of markers, and video contouring prior to storage of the image. Each of the memories contains a 248 x 255 array with a four-bit code to represent the color and/or intensity of individual points. In addition, the contour threshold colors and levels as well as parameters such as antenna angle, marker spacing, and time are presented within a 248 x 70 ancillary data area along the right edge of each picture.

The image data in any of the four memories of the Master Scan-Converter Refresh Memory can, upon manual initiation, be accessed, combined with appropriate synchronization codes, and serially transmitted to a Remote Refresh Memory via a 2400 bit/second telephone line. Conventional CRT alphanumeric display terminals, located with both the

master and remote systems, communicate with each other over the same line.

The Display Data Interface permits manual or automatic transfer of image data between the refresh memories and an external minicomputer. A trackball-positioned cursor enhances operator interaction with both the scan converter and the computer.

Time-division multiplexing of the memory buss among the four display channels in the Master Scan-Converter Refresh Memory permits different operations to be accomplished simultaneously in different channels. For example, it is possible to coordinate-convert, contour, and store radar video in one channel, while transmitting image data from another channel to the Remote unit and interacting with the computer in a third channel.

## SECTION 2. GENERAL DESCRIPTION

The block diagram presented in Figure 2-1 should be referred to while reading the following description of the system.

### 2.1 Master Scan Converter and Refresh Memory

#### 2.1.1 Scan Conversion Processor

Front panel controls related to scan-converter operation are located on the Scan Conversion Processor and are connected to various cards within it as shown. The Scan Conversion Processor accepts synchro or binary inputs for antenna azimuth and elevation angles as well as video and timing signals from a radar signal processor. The input information is converted in real time from its polar form to a rectangular form suitable for entry into the image-oriented memories. The processor also generates all multiplexed memory addresses, timing, and control signals needed by the memory-interface units, plus alphanumeric data and color patches.

Located within the processor is a SDF (Serial Data Formatter) which, upon manual initiation through the Data Transmission Control Panel, generates memory addresses sequentially and accepts the corresponding data from any memory.\* Interleaved with appropriate synchronization codes, the resultant serial data output drives an external MODEM. The SDF operates in bit synchronism with a clock from the MODEM; at a 2400 kHz clock rate, the transmission of one image takes about 2.7 minutes. Capability for two different self-test modes has been built into the SDF.

The SDF also accomplishes multiplexing of data to and from a CRT alphanumeric display terminal. Whenever a display image is not being transmitted by the SDF, the MODEM input is made available to the terminal's keyboard. The MODEM data output is dedicated to the CRT alphanumeric display, thus allowing the remote operator to communicate to the data originator even during display image transmission.

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\*Within a given channel, video storage has priority over transmission.



Within the Scan Conversion Processor is a Display Data Interface (DDI) which permits communication between the Scan Converter and a Universal Logic Interface (ULI) of an Interdata 7/32 minicomputer. The minicomputer treats the Scan Converter as a peripheral and can perform data transfers to and from its refresh memories.\* A cursor can be switched on in any display, its position adjusted, and the four-bit color code in the refresh memory at that position transmitted to the computer by operator interaction through the Display Interface Control panel.

#### 2.1.2 Memory Interface Units

Each MIU (Memory Interface Unit) performs parallel-to-serial and digital-to-analog conversions on its memory output to generate red, green and blue video signals for the corresponding display. These units also execute code conversion and contouring on the incoming video as a function of color patches and contour levels stored in the associated memory. Intermediate storage and logic in each MIU enables it to alter data in its memory as commanded by the Scan Conversion Processor.

#### 2.1.3 Memories

The image storage media are conventional AMPEX magnetic core memory systems having 8192 40-bit words for each display. They have split cycle times of 750 nanoseconds and self-contained power supplies which also power each associated MIU. Data sheets are included in Appendix A.

#### 2.1.4 Displays

The displays are 19-inch CONRAC delta-gun color units of the type used as monitors in television studios. Each unit has red, green and blue video inputs driven by its MIU. All of the displays are synchronized by the same H and V drive pulses from the Scan Conversion Processor. Data sheets for the monitors have been included in Appendix A.

#### 2.1.5 MODEM

The 2400 bit-per-second synchronous MODEM provides bi-directional data communication with the Remote Refresh Memory over an unconditioned

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\*In each channel, video storage and transmission have priority over most DDI operations.

four-wire Type 3002 private line. A 2400 Hz clock from the MODEM drives both the SDF and the CRT terminal. A data sheet for the General Data Comm Industries, Inc. GDC 201-9 MODEM, along with a table describing the jumper positions and control settings necessary for direct four-wire connection to the remote unit, are included in Appendix A.

#### 2.1.6 CRT Alphanumeric Display Terminal

The Infoton VISTAR/GT terminal has a CRT Alphanumeric Display with refresh memory to store up to 24 lines of 80 characters each received either from its own keyboard or from that of the remote unit. The terminal operates in half-duplex mode on an external clock supplied by the MODEM. A data sheet is included in Appendix A.

### 2.2 Remote Refresh Memory

#### 2.2.1 Remote Refresh Memory Receiver

On the front panel of this drawer are mounted all controls needed for normal operation of the RRM (Remote Refresh Memory). The only circuit card within the receiver drawer is the DRU (Display Receiver Unit) which is the heart of the RRM. The DRU detects synchronization codes within the incoming data signal and generates all memory addresses, timing, and control signals needed by the MIU (Memory Interface Unit). It also generates a simulated data signal for test purposes and interfaces the CRT Alphanumeric Display Terminal with the MODEM.

#### 2.2.2 Memory Interface Unit

The MIU used in the RRM is of the same basic design as that described in section 2.1.2, except that the code-conversion and contouring functions are excluded and the memory-address-buss timing differs.

#### 2.2.3 Memory

See 2.1.3

#### 2.2.4 Display

See 2.1.4

2.2.5 MODEM

See 2.1.5

2.2.6 CRT Alphanumeric Display Terminal

See 2.1.6

## SECTION 3. OPERATION

### 3.1 Master Scan Converter and Refresh Memory

#### 3.1.1 Display Adjustment

Each monitor should have its CH A/CH B switch in the CH A position for normal viewing. The INT SYNC/EXT SYNC switch was disabled in the process of modifying the monitors to operate with separate H and V external sync. signals.

The BRIGHTNESS control should be used to set the black background level (observe the area around the alphanumerics) to a point near the threshold of visibility. The CONTRAST control can then be used to obtain the desired intensity. The illuminated number at the bottom of each monitor is red when information is being stored in its memory.

#### 3.1.2 Contour Threshold Entry

The contour threshold switches are arranged in the same pattern on the front panel of the Scan Conversion Processor (see Figure 3-1) as on the actual displays. Any of the 15 color-selectors can be set to any color between 0 (black) and 15 (red). \* The 14 level-switches should be set up in ascending magnitude order from bottom to top. An area of the display will take on a color of a given patch if the corresponding signal processor output is equal to or greater than the level below the patch and less than the level above the patch. Should these levels be set to the same number, the color in the patch between them will never appear.

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\* Color 15, however, is reserved for range and altitude markers and has the property of not allowing itself to be written over. Patterns appearing in this color can only be removed by erasure.

# SCAN CONVERSION PROCESSOR

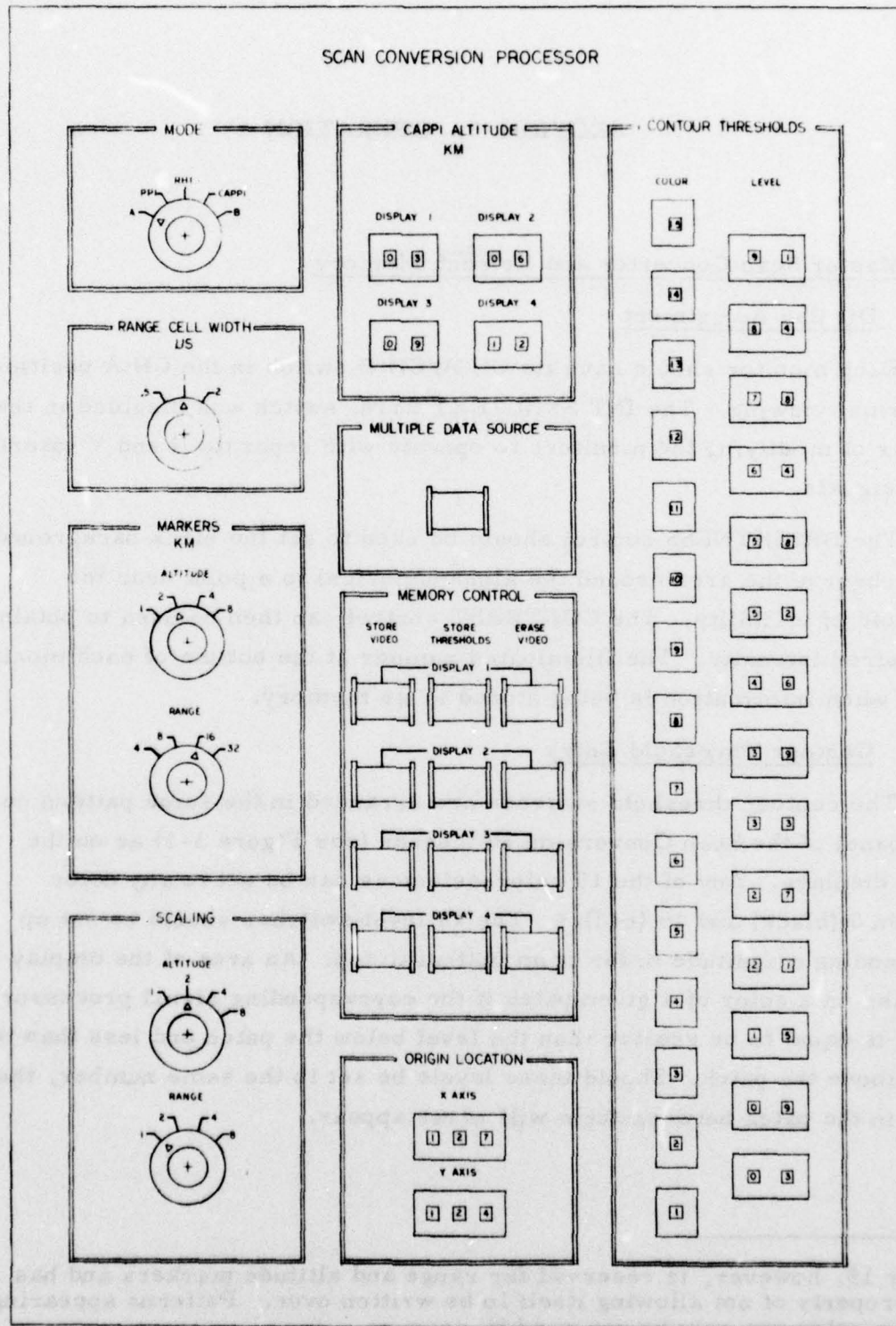


Figure 3-1. Scan Conversion Processor Front Panel

Having set up the contour threshold switches, the operator need only depress the STORE THRESHOLDS button for each display in which this set of contour thresholds is desired. The previous set of thresholds in that memory is then replaced by the new set without affecting the other display information which had been entered using the previous set of thresholds. (This situation, where the thresholds do not match the displayed information, can be avoided by pushing the appropriate ERASE VIDEO button before entering new contour thresholds.) All subsequent incoming video will be contoured according to the new set of thresholds.

### 3.1.3 Mode and Range Cell Width Selection

These controls must be set to correspond with the radar scan sequence and the range cell width of the radar signal processor. Any of the display formats selected by the MODE switch can be set up in any display or combination of displays by depressing the desired STORE VIDEO switches, which are active when lit. When a STORE VIDEO switch is on, the number below the corresponding display is illuminated in red. STORE VIDEO operations have priority over image transmission or computer interface which requires memory addressing within each display channel.

#### 3.1.3.1 THI

MODE switch position A selects the THI (Time-Height Indicator) display format where time is presented along the X-axis and height appears along Y. The letters 'TH' appear in the first line of characters in the parameter area at the lower right of the screen. The display emulates a strip chart recorder's operation, with new data appearing at the right while all other data are shifted left. New data appear always in block 24, the right most block and the one adjacent to the ancillary data area (see Figure 4-8). Its ten points are filled one-by-one until, when they have all been filled, all blocks are shifted left by one entire block and the process of filling block 24 begins again with subsequent data. When all 25 blocks have been filled, the next new data point causes the left most block to be shifted off the end and lost. The display thus contains between 241 and 250 contiguous time cells representing the most recently received data, with

time increasing to the right. Meanwhile, the vertical axis represents altitude just as in the RHI mode.

All counters required for generating the time base and time markers are reset when the MODE switch is not at A and run when it is at A. In THI, the STORE VIDEO switches determine which channels are to receive time-height data; those channels not switched on remain unchanged. Should a selected display not be erased before THI data are stored in it, the old data will gradually be shifted left and lost.

#### 3.1.3.2 PPI

The PPI (Plan Position Indicator) mode yields a plan-view display, with the Y-axis running North-South and the X-axis running East-West. The antenna elevation angle appears in the parameter area after EL to the nearest 0.1 degree.

#### 3.1.3.3 RHI

In the RHI (Range-Height Indicator) mode, the display will present ground range along the X-axis and height along Y. The antenna azimuth angle is shown after AZ, in the parameter area to the nearest degree.

#### 3.1.3.4 CAPPI

The CAPPI (Constant Altitude PPI) mode, permits use of any combination of displays with the CAPPI ALTITUDE switch settings appearing after AL in the parameter area at the lower right of each involved display. In this format, each display represents a PPI at the altitude selected.

#### 3.1.3.5 CROSSHATCH

Mode switch position B is provided as a test position in which a crosshatch is developed for monitor alignment purposes. The crosshatch appears in the color corresponding to full-scale video (the top patch), while the background appears in the color corresponding to zero video (the bottom patch).

#### 3.1.4 Scaling and Location of the Origin

In PPI, RHI or CAPPI modes, the ORIGIN LOCATION switches provide a means of locating the point corresponding to the radar antenna at any position within the display area. The units employed correspond to display elements at (X, Y); (0, 0) is in the upper left corner, while (249, 247) is in the lower right. The center, normally used for PPI formats, is (127, 124).

ALTITUDE (RHI and THI only) and RANGE SCALING switches can be used to vary the scaling as listed in Table 3-1.

Table 3-1.

#### Full Scale Range and Altitude vs Scale Switch Positions (RHI Mode)

<u>SWITCH POSITIONS</u>	<u>1</u>	<u>2</u>	<u>4</u>	<u>8</u>
ALTITUDE	128 KM	64 KM	32 KM	16 KM
RANGE	256 KM	128 KM	64 KM	32 KM

Except for aspects associated with the X-axis, operation in THI is the same as in RHI. The X-AXIS ORIGIN LOCATION switch does not affect the origin location, but its least significant digit is used to select time scaling for the THI mode. If this digit is set to any even number, the normal scaling is selected; otherwise the scaling is 15 times faster. Finer changes in time-axis scaling are obtained by use of the RANGE SCALING switch. The effects of these switches on the time axis are summarized in Table 3-2.

Table 3-2.  
Time-Axis Scaling and Markers (THI Mode)

			# Cells Between Markers (# Markers)			
RANGE SCALING Switch:			<u>1</u>	<u>2</u>	<u>4</u>	<u>8</u>
Seconds/cell:	Normal:*		30	15	7.5	3.75
	Fast:**		2	1	.5	.25
Minutes/250 Cells:	Normal:*		125	62.5	31.25	15.625
	Fast:**		8' 20"	4' 10"	2' 5"	62.5"
<u>RANGE MARKERS Switch</u>	<u>Normal* Minutes/Marker</u>	<u>Fast** Sec./Marker</u>				
32	32	128	64 (3)	128 (1)	256 (0)	512 (0)
16	16	64	32 (7)	64 (3)	128 (1)	256 (0)
8	8	32	16 (15)	32 (7)	64 (3)	128 (1)
4	4	16	8 (31)	16 (15)	32 (7)	64 (3)

\* X-AXIS ORIGIN LOCATION switch set to any EVEN number.

\*\* X-AXIS ORIGIN LOCATION switch set to any ODD number.

### 3.1.5 Marker Spacing Selection

MARKER switches are provided to select ALTITUDE, RANGE, or time marker spacing. In PPI or CAPPI modes, the selected range marker spacing is indicated in kilometers after RM = in the parameter area at the lower right of the display. When the RHI mode is employed, the selected marker spacings are indicated in the display in the following format: M (altitude marker spacing); (range marker spacing) in kilometers.

In the THI mode, the top line of the parameter display area will be TH00M in the normal-scaling case or TH00S in the fast case. The last letter of this line indicates whether the time marker spacing appearing below it has units of minutes (normal scaling) or seconds (fast scaling). The selected marker spacings are indicated in the second line of the parameter

area in the following format: M (altitude marker spacing in kilometers); (range marker spacing in minutes or seconds). In the case where 128 seconds/marker has been selected, the semicolon is replaced by a "1".

#### 3.1.6 Time Code

The lower right corner of each display contains time information in the following format: T (Day of the year); (hour of the day); (minute). The time readout of a particular display is updated only while video information is being stored in the memory of that display.

#### 3.1.7 Multiple Data Source

There are four video inputs to the scan conversion processor. Timing signals for coordinate conversion are derived from radar and range triggers associated with the input connected to J1. When MULTIPLE DATA SOURCE has been selected, the video signals at inputs J1, J14, J13 and J12 are made available for storage on displays 1, 2, 3 and 4, respectively. In the absence of MULTIPLE DATA SOURCE selection, the video input on J1 is made available for storage on all displays.

#### 3.1.8 Image Data Transmission

The DATA TRANSMISSION CONTROL panel is pictured in Figure 2-1. When the MODE switch is in its OFF position, the other two controls are disabled. With the MODE switch in the TRANSMIT position and the TEST CLOCK switch OFF, depressing the START button initiates the transmission of data from the display memory selected by the DISPLAY switch. The START button will light immediately and will remain illuminated until the transmission has been completed. The transmission time duration, in seconds, is given by  $386/f$ , where  $f$  is the clock frequency in kHz. The light will not come on if: 1) the MODE switch is at OFF, 2) the STORE VIDEO switch for the source display is ON, or 3) no clock is present at the Modem Clock Input.

### 3.1.9 Data Transmission Test Modes

Test mode operation is similar to transmit mode operation, except that the serial output is disabled and the time duration is doubled. In TEST A, the image in the source display memory is copied into another memory as follows: 1 to 2; 2 to 3; 3 to 4; 4 to 1. In TEST B, a similar process takes place except that the timing and addresses are scrambled between the source display and the other display so that a pattern corresponding to the line sync. code prefix and line number code appears instead of the image from the source display. If, after running TEST A, both displays are identical, then serial data are correct at a point just before the actual line driver in the SDF. If, after running TEST B, the characteristic pattern (compare with a photo) is observed, then the sync. code prefix and line number code are correct at the line driver input. The test modes can be run much more rapidly without the modem clock by substituting instead the TEST CLOCK selected on the control panel.

### 3.1.10 Display Interface Control

Interaction between an external minicomputer and the display refresh memories is under partial control of the DISPLAY INTERFACE CONTROL panel illustrated in Figure 2-1. Except for the ERASE DISPLAY buttons, all of the switches on the control panel also serve as indicators controlled by their state and/or the DDI (Display Data Interface) within the scan converter. The DISPLAY MEMORY ACCESS controls, when lit, indicate that write and/or read data transfers are enabled in the hardware. If an SDF test mode has been selected, or if either a data transmission or store video is in progress in the display channel last selected by the computer, then these indicators will not be lit. However, DDI operations not requiring memory address access are still possible.

The scan converter ERASE VIDEO buttons used in normal operation do not erase the entire screen; the contour threshold legend area is left unchanged. In addition, a mask obscures from view certain areas within the ancillary data portion of the screen. These areas contain coded information available to the computer and needed by the contouring hardware. The ERASE DISPLAY buttons on the DISPLAY INTERFACE CONTROL panel not only erase

the entire display, but also inhibit the mask so that the entire screen is available to display information from the computer. The mask and the legend are restored when the operator actuates the corresponding STORE THRESHOLDS button on the scan conversion processor.

The cursor can be made to appear in any display by depressing the appropriate CURSOR ON/OFF switch; the on state is indicated by illumination of the switch. The cursor, a blinking single point on the display, can be located anywhere on the screen by means of the CURSOR POSITION trackball. If any SEND DATA indicator is lit, no cursor will respond to the trackball. The cursor changes color as a function of its surroundings so as to remain visible. During normal scan converter operation, the mask will obscure the cursor. If the cursor cannot be found, the following property may be useful: along the Top and Left edges of the display, the cursor will stop even if the trackball is rotated too far. (At the bottom edge, the cursor disappears. When moved beyond the right edge, it reappears at the left where it finally stops about an inch from that edge; however, if the SEND DATA button were pressed with the cursor in such a position, the address would be wrong.)

The color/intensity code covered by the cursor, as well as its coordinates, can be entered into the computer by pushing the appropriate SEND DATA button. The corresponding cursor must be switched ON for this action to be recognized. The SEND DATA switch will light when depressed, if the DDI control logic is in the proper state, and will extinguish about one-half second after the resulting interrupt has been serviced by the appropriately-programmed computer. Pressing the INI button on the analyzer console should always turn off any SEND DATA indicators which are lit for whatever reason. Details on programming the computer which treats the DDI as a peripheral are included in section 4.7.

#### 3.1.11 Interlaced Scan Mode

If, in future applications, there is a requirement to drive a device requiring a standard 525-line interlaced scan, the INTERLACE switch must be turned on. Otherwise, the non-interlaced mode which is better for jitter-free close viewing can be used.

### 3.1.12 Data Save

While turning the POWER switch off, depress the DATA SAVE button next to it. This action will prevent spurious data from entering the memories at turn-off and can be used to save images for indefinite periods of time, since the memories are non-volatile.

### 3.1.13 Alphanumeric Data Transfer

When image data are not being transmitted by the SDF, the CRT alphanumeric display terminal can communicate with its counterpart in the RRM in the normal half-duplex mode. While the SDF is transmitting, alphanumeric data from the RRM will be received by the MASTER unit but transfer in the other direction is not possible.

## 3.2 Remote Refresh Memory

### 3.2.1 Reception of Images

When the operator of the Master SCRM initiates a transmission, the data describing an image are transmitted serially via the MODEMS and data line (see Figure 2-1) to the Remote Refresh Memory display unit. The control panel for the remote unit is shown in Figure 2-1. The "on" state of the RECEIVE switch is indicated by its illumination. The incoming image data are stored in the memory only if the RECEIVE switch is on. Thus, should an image need to be saved, the RECEIVE switch should be turned off to preclude the possibility of its being written-over by new data. An ERASE button is provided to clear the entire display image.

### 3.2.2 Test Mode

When the TEST switch is on, the receiver ignores the normal inputs and instead accepts data and clock signals from an internal test pattern generator. This test, if the correct pattern is observed, verifies proper operation of almost all RRM circuitry--only a multiplexer and the line receivers are not tested. Unlike the one-shot transmission of data from the Master SCRM, the test pattern generator runs continuously. The test pattern is also useful for converging the monitors and adjusting colors.

3.2.3 Interlaced Scan Mode

See 3.1.11

3.2.4 Data Save

See 3.1.12

3.2.5 Alphanumeric Data Transfer

See 3.1.13

## SECTION 4. DETAILED CIRCUIT DESCRIPTION - MASTER SCRM

The descriptions appearing in these sections generally refer to diagrams included among the text. In some cases; however, it might be helpful to refer to the actual schematics. A complete listing of drawings applicable to the third scan converter can be found in AJJ-49 of Appendix C.

### 4.1 Angle Interface Unit

The Angle Interface Unit, located in the upper-rear position of the coordinate converter drawer, accepts synchro azimuth and elevation data in standard  $R_1$ ,  $R_2$ , and  $S_1$ ,  $S_2$ ,  $S_3$  format and converts these data to the following outputs:

Scaled BCD azimuth angle, $1^\circ$ resolution	}	(for parameter area of display)
Scaled BCD elevation angle, $0.1^\circ$ resolution		
Sine/cosine azimuth 13 bits	}	(for coordinate conversion)
Sine/cosine elevation 13 bits		
Elevation greater than $12.65^\circ$ flag	}	(for CAPPI)

Azimuth and elevation synchro inputs are converted to 14-bit binary numbers (MSB =  $180^\circ$ ) in Data Device Corporation synchro-to-digital converters model ESDC-6\*. (These converters are inhibited during sampling by the S/D inhibit command input.) The 14-bit binary outputs are fed both to rear panel connector J3 through line drivers and to multiplexers A21 through A24 and A7 through A10\*\*. These multiplexers select binary-angle data from either a rear panel connector J4 or from the synchro-to-digital converters. They have been provided, should the need arise to drive the

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\* See Appendix A.

\*\* Actually only 12 bits of Azimuth and Elevation are included in J3 and J4 at the rear panel; the two additional elevation bits, both input and output, are connected to J2 - See 897392.

system from a digitally generated angle source. If J4 is not connected, the multiplexer select line is pulled up so that the converter outputs are selected.

Binary-angle data are next converted to sine and cosine in an Interface Engineering sine/cosine controller model 109 and angle-to-sine converter model 108\*. The controller adapts the angle-to-sine converter to full four-quadrant sine and cosine operation. A logic zero on the controller input terminal 23 selects sine. The sine/cosine converter channel is multiplexed once each PRF interval between azimuth and elevation inputs through multiplexers A16 through A18.

An Interface Engineering binary angle to scaled BCD converter, model 107\*, provides the drive for the antenna angle readout in the parameter area of the display. This converter is switched between azimuth and elevation by multiplexers A11 through A14, controlled by the front panel mode switch. Azimuth is displayed in the RHI mode; while elevation is displayed in PPI and CAPPI modes.

Multiplexers A3, A4 and A5 line shift the scaled BCD four lines down when displaying elevation to provide the increase in resolution from  $1^\circ$  to  $0.1^\circ$ .

The magnitude comparators, A20 and A25, generate a logic one when the antenna elevation angle exceeds  $12.65^\circ$ . This output is used by the coordinate converter in the CAPPI mode to initiate the  $2^\circ$  elevation step.

#### 4.2 Coordinate Converter

The Coordinate Converter derives the cartesian memory address from the radar parameters of elevation angle, azimuth angle, radar trigger and the range gate clock. The azimuth angle and elevation angle are sampled once every radar period to form the basis of the coordinate transformation. The block diagram of the Coordinate Converter unit is shown in Figure 4-1.

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\*See Appendix A.

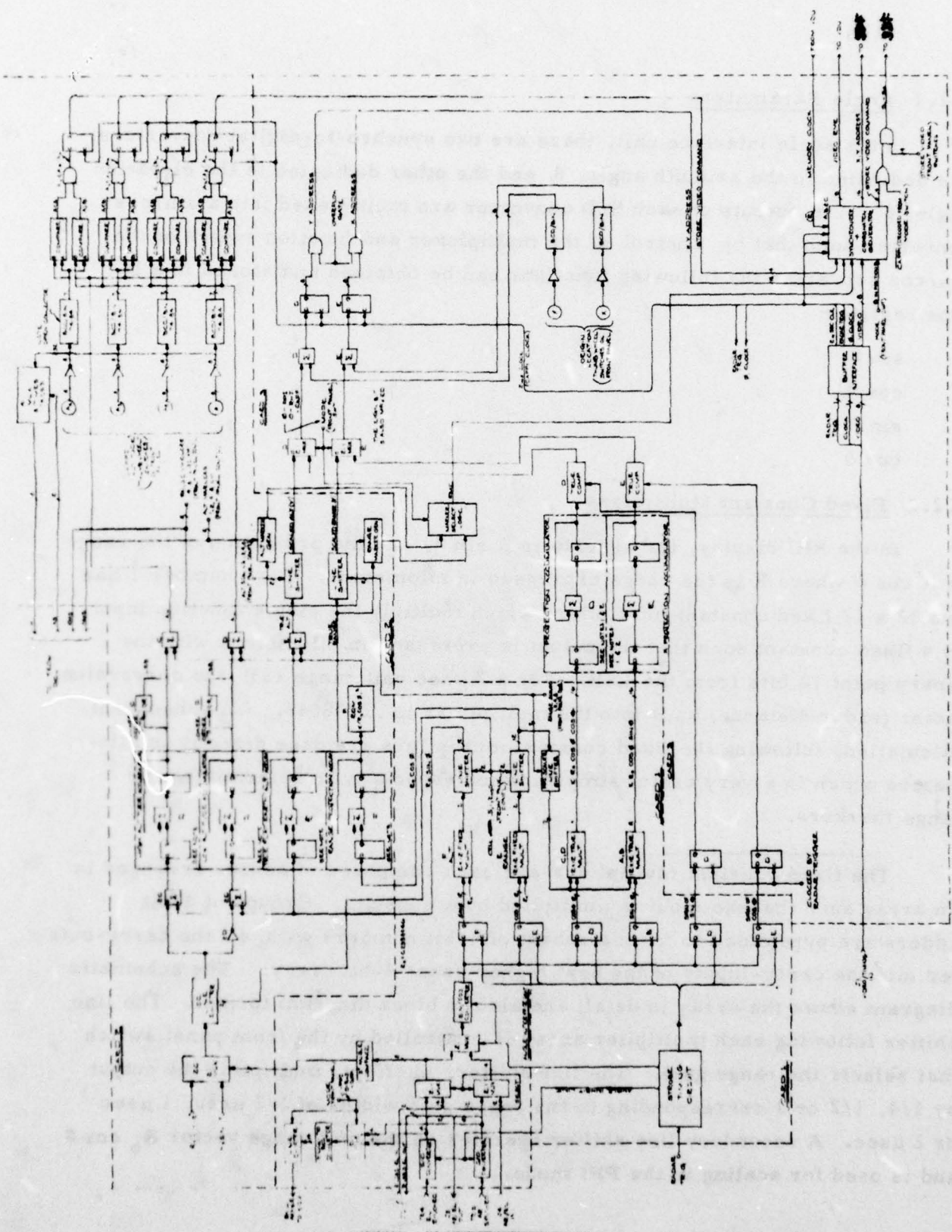


Figure 4-1. Coordinate Converter Block Diagram

#### 4.2.1 Angle Parameters

In the angle interface unit, there are two synchro-to-digital converters: one dedicated to the azimuth angle,  $\theta$ , and the other dedicated to the elevation angle,  $\phi$ . The outputs of each S/D converter are multiplexed into a sin/cos converter such that by control of the multiplexer and function switch of the sin/cos converter, the following functions can be obtained and stored in a D type register:

sin  $\phi$   
cos  $\phi$   
sin  $\theta$   
cos  $\theta$

#### 4.2.2 Fixed Constant Multipliers

In the RHI display, the altitude is  $R \sin \phi$ , and the projection of the range is  $R \cos \phi$  where  $R$  is the range expressed in kilometers. Card number 1 has two  $12 \times 12$  fixed constant multipliers which multiply the single function input by a fixed constant such that the output is expressed in kilometers with the binary point 12 bits from the LSB. For a  $2 \mu\text{sec}$  unit range cell, the conversion factor (radar distance) built into the multipliers is .2998046. All subsequent calculations following the fixed constant multipliers are done directly in kilometers which is a very useful simplification especially in determining the range markers.

The fixed constant multipliers are each composed of adders arranged in an array such that the input is multiplied by a constant. Groups of 4-bit adders are pyramided to form a subset of 4-bit numbers with all the carry-outs fed into the carry-inputs of the next higher order 4-bit array. The schematic diagram shows the array in detail and also in block diagram format. The line shifter following each multiplier array is controlled by the front panel switch that selects the range gate. The line shifter, in effect, multiplies the output by  $1/4$ ,  $1/2$  or  $1$  corresponding to the range gate widths of  $1/2 \mu\text{sec}$ ,  $1 \mu\text{sec}$  or  $2 \mu\text{sec}$ . A secondary line shifter operates on the unit range vector  $R_0 \cos \phi$  and is used for scaling in the PPI mode.

#### 4.2.3 PPI Mode - True 12 x 12 Multipliers

In the PPI mode, the projected range,  $R_o \cos \theta$ , is broken up into its X (East-West) and Y (North-South) coordinates. The azimuth angle  $\theta$  is measured from the North-South line such that

$$X_o = R_o \cos \phi \cos \theta$$

and 
$$Y_o = R_o \cos \phi \sin \theta$$

Since  $R_o \cos \phi$  had already been established in one of the fixed constant multipliers, two other multipliers are used to establish  $X_o$  and  $Y_o$ , the unit component vectors for the PPI display.

The 12 x 12 true multipliers consists of an array of partial product terms added in a pyramid structure very similar to the fixed constant multiplier. The partial product terms and summation pyramid are detailed in the schematic drawing of the 12 x 12 multipliers.

Card 2 of the coordinate converter thus develops the unit altitude  $R_o \sin \theta$ , the unit range  $R_o \cos \phi$ , and the component vectors of the unit range  $R_o \cos \phi \cos \theta$  and  $R_o \cos \phi \sin \theta$  all evaluated in kilometers.

#### 4.2.4 Address Accumulators - Card 2 and Card 3

The unit coordinates have been derived for the first range cell. Coordinates for other range cells can be easily obtained by taking advantage of the fact that the range cell number increases linearly in a radar. Thus, the coordinates for range cell  $j + 1$  are the coordinates for range cell  $j$  added to the value of the respective coordinates of range cell 1. This accumulator type structure is shown in the block diagram and is repeated 6 times in the coordinate converter. The unit vectors are loaded into each accumulator at the beginning of each radar period and at the same time the old data is cleared out. The accumulator is clocked by the range gate clock of the integrator to form the cartesian coordinate addresses.

For the RHI mode of operation, the Y address corresponds to the scaled altitude and the X address is the scaled range. For the PPI or CAPPI mode of operation, the Y address corresponds to the North-South component of the range vector and the X address corresponds to the East-West component of the range vector. The mode switch controls the multiplexer to select the appropriate coordinates as shown in the block diagram. After the multiplexer, constants controlled by thumbwheel switches can be added independently to the X and Y coordinates to affect translation in both directions. A hard limiter circuit is used to prevent overflow and erroneous addresses.

#### 4.2.5 Range and Altitude Markers

The outputs of both the range and altitude accumulators are in kilometers (see para. 4.2.2) i.e., the 13th bit is 1 KM, the 14th is 2 KM, etc. Detection of the clock cycle at which time the bit corresponding to a preselected range changes state is used as the marker pulse. The circuitry consists of comparing the selected bit with the same bit delayed one clock period in an exclusive or circuit to form the marker pulse. The marker pulse goes through the synchronizer to produce the range mark enable (RME) signal. Range markers are disabled in THI so that elevation angles other than  $90^\circ$  can be used without spurious marker problems.

#### 4.2.6 CAPPI Mode

In the CAPPI mode, the antenna sweeps  $360^\circ$ , or a segment thereof, at a single elevation angle and upon reaching its starting or terminal position (for less than  $360^\circ$  sweep) the elevation angle is incremented and the process is repeated. A typical CAPPI will use the following elevation angles, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, 16, 18 and  $20^\circ$ . This volume scan permits the operator to crudely establish a map of a prescribed altitude or many altitudes, since, in general, each radar beam will pass through all possible altitudes. By carefully selecting and storing the incoming data, it is possible to develop a constant altitude PPI map at any given altitude. Because the elevation angle of the antenna is incremented in small steps, a map at precisely the desired elevation would provide very few sample points; it is the established procedure to sample the elevation at or near the desired elevation.

Figure 4-2 shows a constant altitude intersecting three different angle vectors or rays. The solid lines represent the CAPPI elevation angles and the dotted lines represent elevation angles between the CAPPI rays. For elevation angle  $\phi_j$ , information is recorded when the altitude reached by the altitude vector associated with the ray at  $\phi_j + 1/2$  is equal to the preselected altitude, similarly the data recording is stopped when the altitude reached by the altitude vector associated with the ray at  $\phi_j - 1/2$  equals the preselected altitude. From the diagram, it can be seen that there are no gaps in obtaining all the altitude information for a preselected altitude as the beam increments discretely in elevation angle.

In the coordinate converter, the altitude is developed in the altitude accumulator from the unit altitude vector  $R_0 \sin \phi$ . A unit high altitude vector  $R_0 \sin (\phi + 1/2)$  and a unit low altitude vector  $R_0 \sin (\phi - 1/2)$  are also developed and introduced into their respective accumulators to form the high and low altitude addresses respectively,  $A_H$  and  $A_L$ .

For small angles, the approximations

$$\sin (\phi + 1^\circ) \approx \sin \phi + \sin 1^\circ$$

and

$$\sin (\phi - 1^\circ) \approx \sin \phi - \sin 1^\circ$$

were used.

The selection criteria for a preselected altitude  $A_j$  is the following:

$$A_L \leq A_j \leq A_H \quad ; \text{ store data in } j^{\text{th}} \text{ memory}$$

For each altitude, two comparators are used and are shown in the diagram of card 2.

#### 4.2.7 Coordinate Converter/Integrator Interface

The Coordinate Converter is slaved to the integrator by using the radar trigger and range gate clock from the integrator. Synchronization between the Coordinate Converter and the integrator is the major reason for slaving the coordinate converter to the integrator. However, synchronization is not sufficient in order to format data rates greater than 0.6 MHz, the fastest data

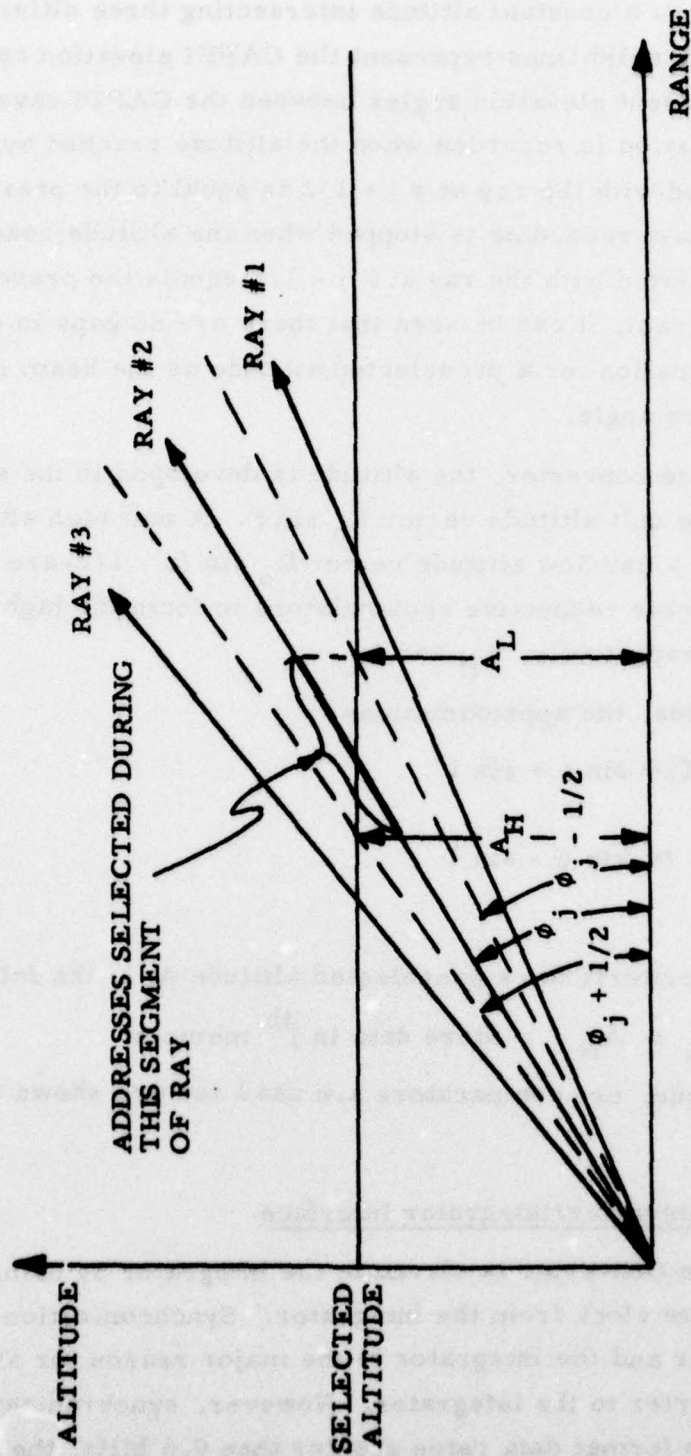


Figure 4-2. CAPPI Address Selection

rate the memories can accept. For instance, it would be impossible to accept  $1\ \mu\text{sec}$  range gates directly from the integrator, but it is possible to receive alternate  $1\ \mu\text{sec}$  range gates from the integrator during one radar period and the previously non-selected  $1\ \mu\text{sec}$  range gates during the second radar period. This is possible because the integrator has holding loops already built into its output circuitry and, simply by selecting the starting range gate in a sequence, it is possible to store all of them.

A simple block diagram and timing waveform is shown in Figures 4-3 and 4-4. The radar trigger passes through a modulo 2 and modulo 4 counter. The output of the counter controls a multiplexer, the inputs of which are gate pulses that start on either the first, second, third or fourth pulses. These gate pulses are used to gate the range gate clock that ultimately drives the accumulators. The coordinate addresses are strobed by means of a  $2\ \mu\text{sec}$  clock into the synchronizer. The  $2\ \mu\text{sec}$  clock is also derived from the gated range gate clock and a modulo n counter where n depends on the range gate width.

#### 4.2.8 Synchronizer

The Coordinate Converter and the memory unit run on independent clocking signals and the synchronizer is the means for interfacing these two asynchronous systems. The memory can accept data at a rate not to exceed 0.6 MHz, and the synchronizer will work at any input data rate provided the maximum 0.6 MHz rate is not exceeded.

The synchronizer input data consist of 8 bits each of X, Y and video information, RME, and 4-bits of memory select information(the store commands). Since these 29 bits come in parallel, operation of the synchronizer can be understood by considering a single bit. Figure 4-5 is a simplified block diagram of the synchronizer and the timing waveforms showing the operation of the system. Incoming data are stored in one of two D-type registers such that each DATA BIT is stored for 2 clocking cycles. The purpose of the synchronizer is to insure that the data are "good", i.e., there is no chance of a data edge or change during the time that the memory clock strobes out the

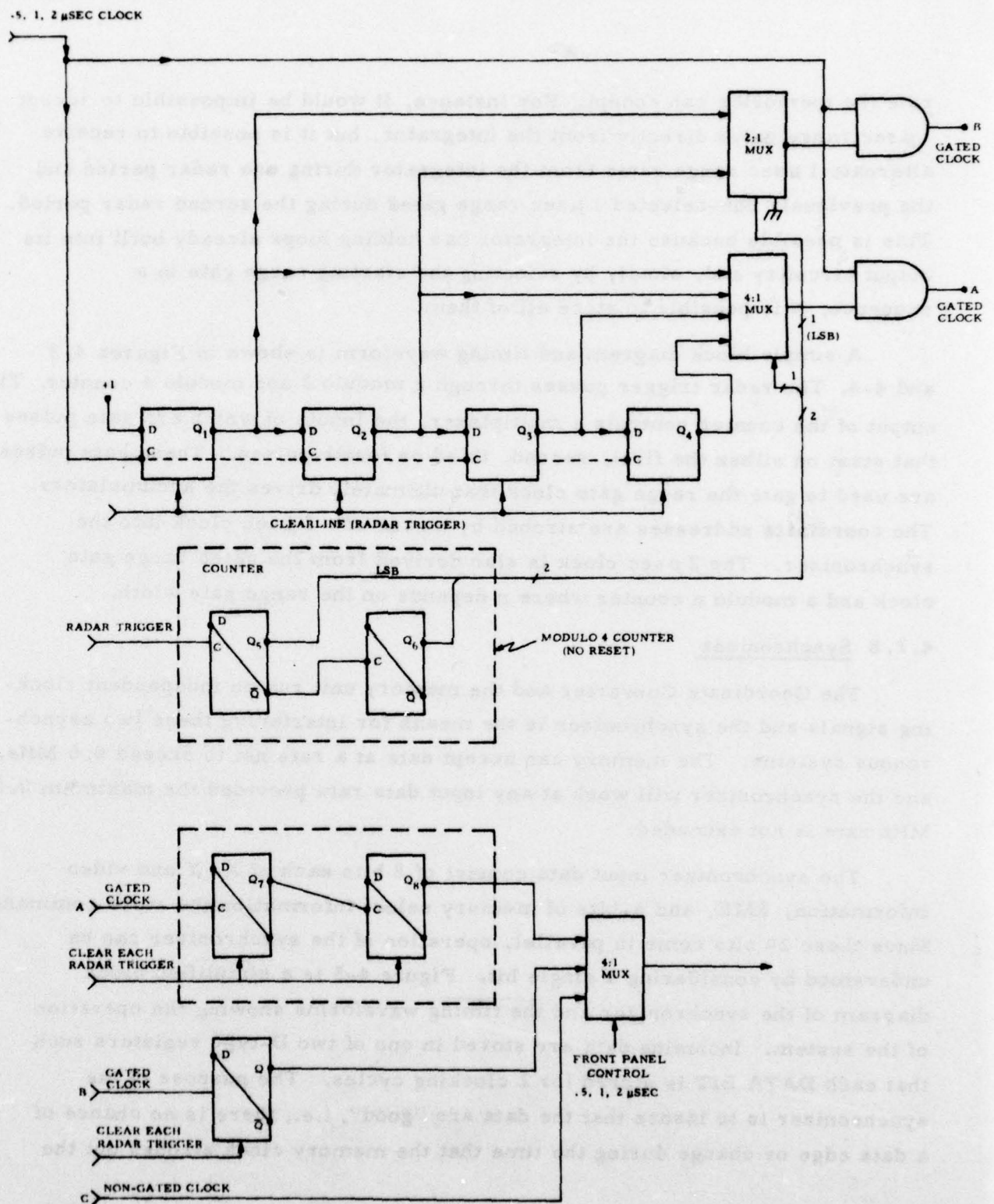


Figure 4-3. Timing Interface for Coordinate Converter and Integrator

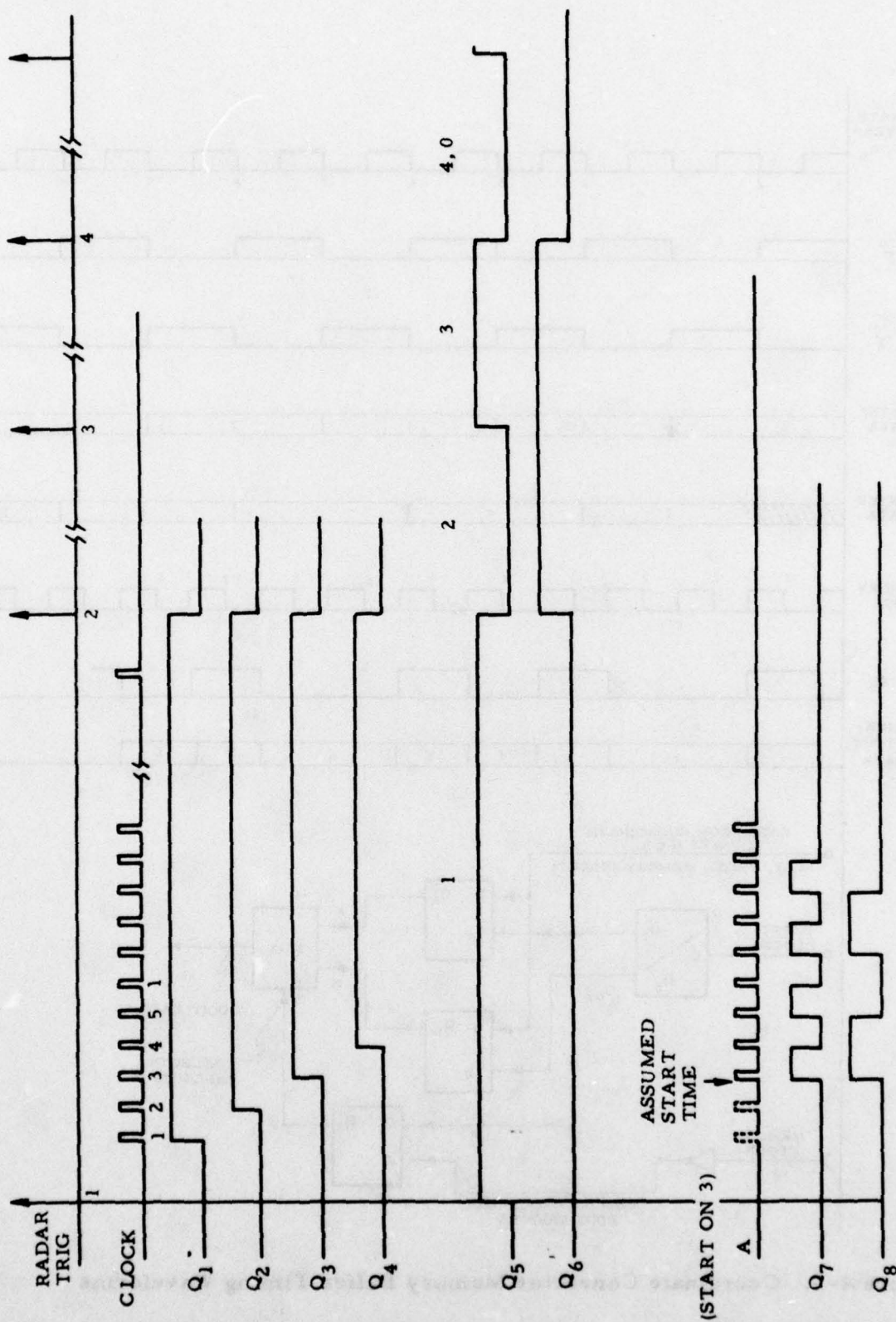


Figure 4-4. Integrator Coordinate Converter Timing Waveforms

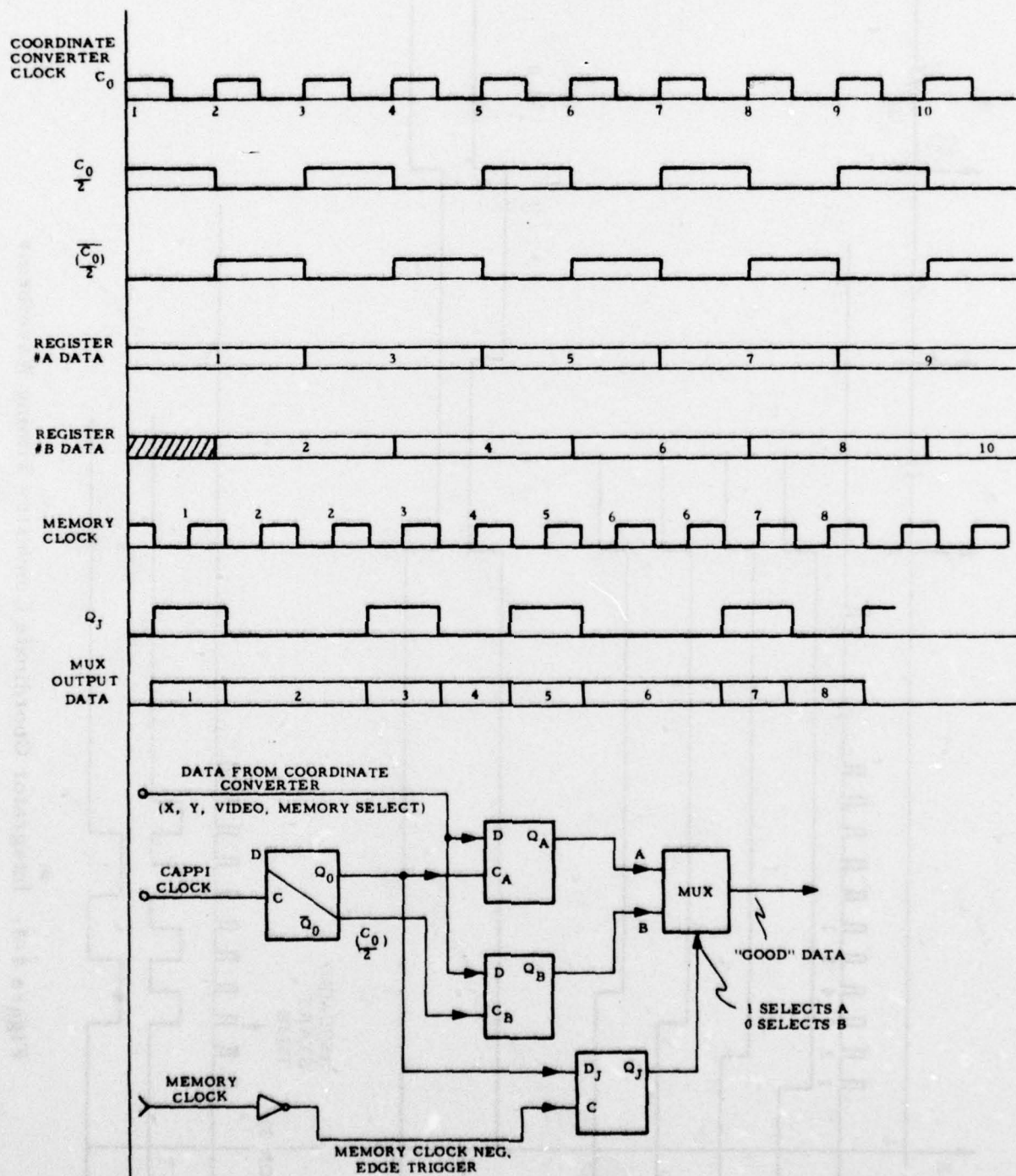


Figure 4-5. Coordinate Converter Memory Buffer Timing Waveforms

data. It can be shown that at least one of the data inputs to the multiplexer will not change during the strobe time (pos. edge) of the memory clock. By strobing ( $\frac{C_o}{2}$ ) into a D-EDGE register using the negative edge of the memory clock will provide an output signal  $Q_j$  that can control the multiplexer to select the signal that is guaranteed to be "good" by the time that the positive edge of the memory clock comes along. Notice that there can be an ambiguity in  $Q_j$  itself, i.e., assume ( $\frac{C_o}{2}$ ) is changing at the time the negative edge of the memory clock arrives. This ambiguity, however, does not produce an ambiguity at the time the positive edge of the memory clock arrives, for regardless of which register was selected by the multiplexer, the data in either register cannot change for  $2 \mu\text{sec}$  (the  $C_o$  clock period) and the data will be strobed out in  $.8 \mu\text{sec}$ , hence, the data will be good.

If on the other hand, we look at the situation in which the data are changing in one of the storage registers at the time of a positive going edge of the memory clock, we find that the multiplexer always selects the other register. Data can be clocked out twice as shown in the example (data #2 and #6), but will cause no problems in the system since it implies that the same data will be reentered at the same memory location, causing no change. The synchronizer is on card 3. Additional bits of the synchronizer, located on the VDU card to be described, operate on the three additional video inputs enabled by the MULTIPLE DATA SOURCE switch.

#### 4.2.9 Angle Interface Timing

On card 1 is the angle interface timing which operates the control lines of the multiplexer and the control line of the sin/cos converter as well as providing an inhibit line for the S/D converters. At the start of each radar period, a gated delay line oscillator is turned on and drives a counter. The counter is decoded to derive the approximate control line code to obtain the desired function of either  $\sin \theta$ ,  $\cos \theta$ ,  $\sin \phi$  or  $\cos \phi$ . When this function is available, it is strobed into the appropriate D-register shown in the block diagram.

This is done only once every radar period. The input to the coordinate accumulators are those unit vectors that have been determined on the previous radar period.

#### 4.2.10 Earth Curvature Correction

A correction term is added to the altitude address to correct for earth curvature. This correction term is a positive function that depends on the flat earth range. A ROM (see Appendix B) is used to obtain the correction factor from the range. A derivation of the correction term is shown in Figure 4-6.

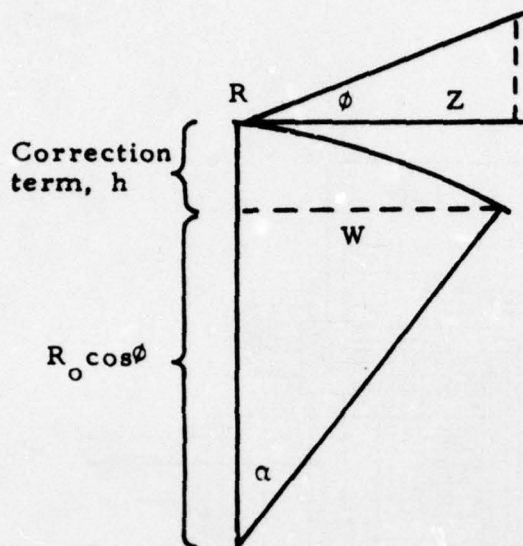
#### 4.3 Display Control Unit

The DCU card contains circuitry which generates all internal timing signals required by the other SCRM cards, the color displays and the memories. The memory control signals which command the core memory modules to perform various functions are developed on the DCU. The ancillary data for all four display channels, including color patches and alphanumeric characters, are generated by the DCU.

##### 4.3.1 Timing and Control Logic

Figure 4-7 presents the DCU block diagram, where it can be seen that all timing waveforms are obtained by frequency division of the 11.958041 MHz crystal controlled clock. Discussion of the outputs of the clock generator, except for R, is postponed until the section on the MIU where these signals are used.

The square-wave R, with a period of 1.6725 microseconds, is illustrated along the X axis of Figure 4-8, which shows the display format along with waveforms. Along the X-axis, the display is organized into ten-point blocks designated DXB0 through DXB31; each period of R corresponds to one block. Since each point requires four-bits for color/intensity coding, 40 bits are needed to specify each block. A memory with 40-bit words has been chosen so that one word in the memory represents each block, 32 words at consecutive addresses describe a line, and 8192 words contain the entire image.



$$h = R_0 - R_0 \cos \alpha = R_0 (1 - \cos \alpha)$$

where  $R_0$  is radius of the earth.

But for small angles,

$$\cos \alpha = 1 - \frac{\alpha^2}{2} \dots \text{hence, } h = R_0 \left( \frac{\alpha^2}{2} \right)$$

Also for small angles  $\alpha \approx \frac{W}{R_0}$

$$h = R_0 \left( \frac{W}{R_0} \right)^2 \frac{1}{2} = \frac{W^2}{2R_0}$$

Note:  $R_0 = 3900$  smi  
(6275.1Km) used in  
ROM Program.

But  $W = R \cos \phi$

$$h \approx \frac{(R \cos \phi)^2}{2R_0} = K (R \cos \phi)^2$$

Figure 4-6. Earth Curvature Correction Term



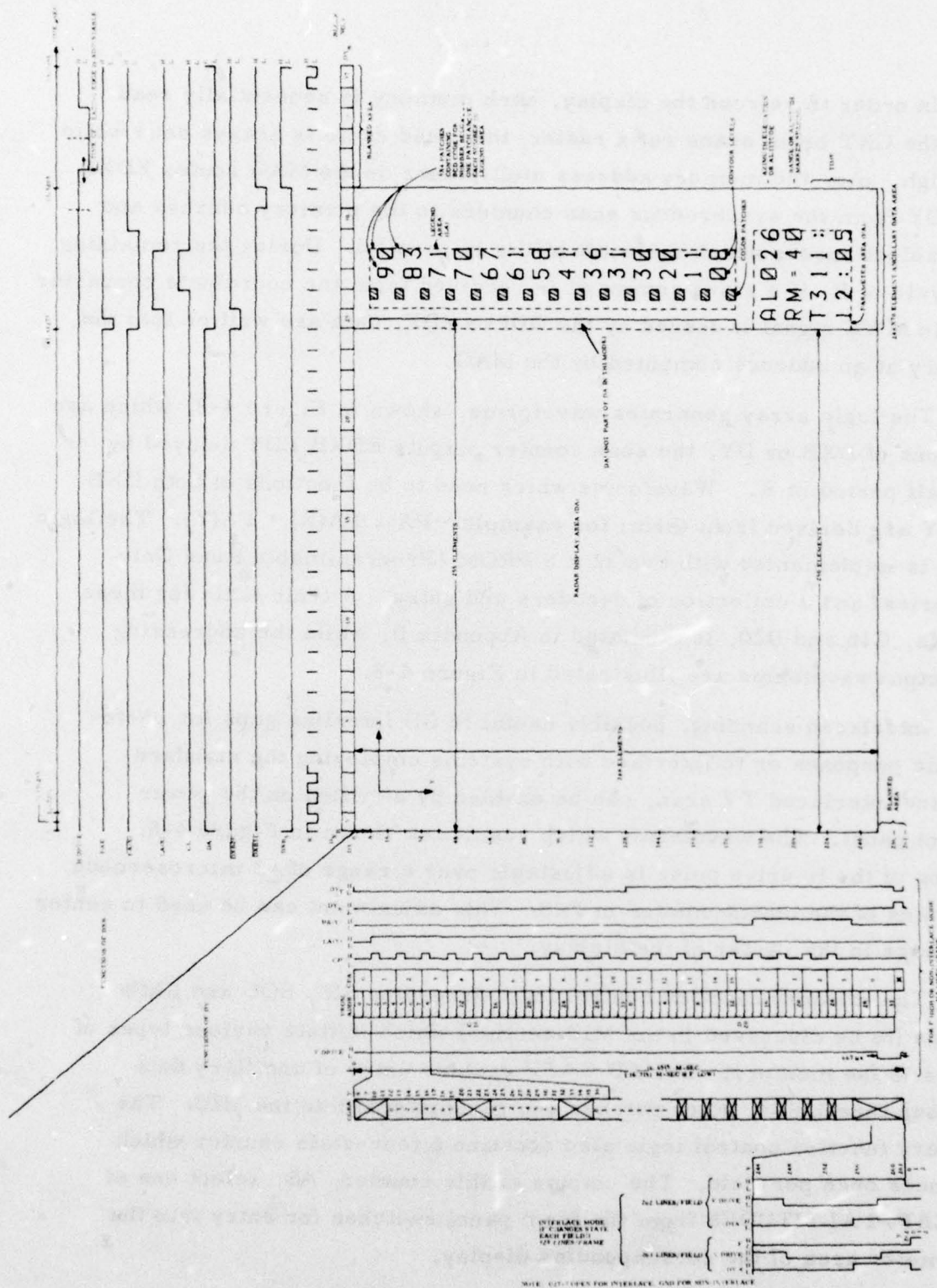


Figure 4-8. Display Format and Timing Diagram

In order to refresh the display, each memory is sequentially read while the CRT beam scans out a raster; this read cycle is always done while R is high, after the memory address multiplexer on the MAG routes EDXB and EDY from the synchronous scan counters to the memory address and point-select busses which drive all MIU's in parallel. During the remaining half cycle of R, if a store command is received from the coordinate converter or if an MWE signal is issued by the DDI or SDF, data are written into the memory at an address computed by the MAG.

The logic array generates waveforms, shown in Figure 4-8, which are functions of DXB or DY, the scan counter outputs EDXB, EDY delayed by one-half period of R. Waveforms which need to be functions of both DXB and DY are derived from them; for example:  $PA = PA(X) \cdot PA(Y)$ . The logic array is implemented with two 32 x 8 PROM (Programmable Read Only Memories) and a collection of decoders and gates. A truth table for these PROMs, C16 and D20, is tabulated in Appendix B, while the addressing and output waveforms are illustrated in Figure 4-8.

Interlaced scanning, possibly useful to fill interline gaps for photographic purposes or to interface with systems employing the standard 525-line interlaced TV scan, can be enabled by a switch on the power control panel. The waveforms which result are shown in Figure 4-8. Timing of the H-drive pulse is adjustable over a range of  $\pm 3$  microseconds by means of the potentiometer in F28. This adjustment can be used to center the image in the raster of the display.

The memory function control logic generates SIC, SOC and RMW signals (to be discussed in the MIU section) which initiate various types of cycles in the memory. The AD GATE enables entry of ancillary data (contour thresholds, color patches and parameters) into the MIU. The memory function control logic also contains a four-state counter which advances once per field. The outputs of this counter, AS, select one of the CAPPI ALTITUDES from the front panel switches for entry into the parameter area of the corresponding display.

The erase logic generates properly times ZID signals which cause all zeroes (black) to be written into the memory at all addresses in response to an ED signal from the DISPLAY INTERFACE CONTROL panel, or at all but the legend-area addresses in response to an ER signal. For use in the THI display format, the erase logic is also designed to permit the following operation when BERD is low. For those channels with their STORE VIDEO switches on, during block 24 time only, the data accessed for refresh are erased. By holding BERD low for at least one complete raster scan, what appears as block 24 on the display can be erased.

The decimal point required in the elevation angle is located in point two, whereas all other ancillary data fall into points five through nine; hence, the decimal point requires a separate signal developed by the DPE generator. The RLS signals, needed by the DDI, are simply the outputs of the STORE THRESHOLDS buttons clocked by DY8 (one per field).

#### 4.3.2 Ancillary Data Formatter

In order to minimize wiring complexity of the array of contour threshold switches, encoding diodes are mounted on the switches themselves as indicated in Figure 4-7. One switch at a time is selected by CP1 through CP15 (CPA decoded, see Figure 4-8) as the display raster is scanned. The color switch outputs are applied to the AD BUSS (a 20-bit buss through which ancillary data can enter points five through nine of any block in memory) when the CRT scan is located in the color patch areas. Similarly stored above each number in the legend area is a patch containing a BCD code for that number. The contour generator to be described in the MIU section and the computer interacting through the DDI make use of these codes which are not visible on the display because a MASK waveform is applied to the MIU. The numbers themselves are generated in a row-select five-by-seven alphanumeric character generator ROM (see Appendix B) which outputs five bits in parallel to a character color encoder. This encoder generates a jumper-programmable four-bit code, now set up as green (0111) or black (0000) for each of the five points.

The ancillary data (angle, altitude, marker spacing and time) are entered into the character generator at the proper time by an array of multiplexers. The mode lines, from the front panel mode switch via the angle interface unit, drive a mode decoder which controls the multiplexers and applies the proper alphanumeric identifiers; AZ, EL, AL, TH, S, M, RM or T which are hard wired. Origin location and range/altitude scaling information is stored only in two unique color patches (see Appendix C, AJJ-21, Figure 3) and not as alphanumerics.

Signals appearing on the AD BUSS or on DPE are not displayed directly, even though they are synchronous with the raster scan format. Rather, the data are stored in the memory when appropriate store commands are issued. Only the memory contents themselves are displayed.

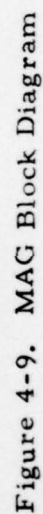
#### 4.4 Memory Address Generator

The principal function of the MAG card is to time-multiplex the 13-bit MA (Memory Address) and 4-bit XP (Point Select) busses, which are daisy-chained through the four MIUs (see Figure 2-1). This multiplexing provides the equivalent of independent memory busses for each of the display channels, thereby permitting simultaneous operations in different channels. For example, it is possible to contour and store video data in one channel while writing from the computer (through the DDI) in another and transmitting (by means of the SDF) from yet another channel. The MAG also provides time-base generation and address processing required in the THI mode.

##### 4.4.1 Time-Multiplexed Memory Address Buss

The MAG block diagram in Figure 4-9 contains priority logic implemented with a PROM (see Appendix B for U28 on MAG) which establishes the following intra-channel priority:

1. Coordinate converter (store video)
2. SDF (image transmission)
3. DDI (computer interaction which requires memory address buss)



The outputs  $AAS_K$  and  $TAS_K$  (where  $1 \leq K \leq 4$  denotes the display channel), when multiplexed by the high-speed clocks A and B from the DCU, select the appropriate source for application to the IX, IY inputs of the MAG during each time slot (see the timing diagram in Figure 4-10). Although each time slot is only 167 nsec wide, use of twisted-pair transmission lines and Schottky logic in critical paths ensures adequate margins. The select lines AASM and TASM drive multiplexers on the DDI and SDF, respectively, to connect the MAG input register inputs IX, IY to each possible address source as follows:

1.  $AASM = 0, TASM = 0$ : SX, SY (coordinate converter)
2.  $AASM = 0, TASM = 1$ : TX, TY (SDF)
3.  $AASM = 1, TASM = X$ : XA, YA (DDI)

The 8-bit X output of the MAG input register is converted in a Schottky CODE CONVERSION PROM (MAG D8, D9 in Appendix B) to the 5-bit block-select code IXB and the 4-bit point-select code IXP. As is described in the MIU section, IXB is concatenated with IYB to form the 13-bit memory address, while IXP selects which of the ten points in the addressed block will be changed.

In THI, the hard-wired number 24 takes the place of the PROM IXB outputs, while BXP from the time base generator (to be described later) appears on IXP. IXP is clocked into another register which, through a buss driver, becomes the actual XP buss. Meanwhile, IXB and IYB are selected by a multiplexer during  $\bar{R}$ --this may seem backwards since these addresses are needed during  $\bar{R}$ , but a look at Figure 4-10 will explain that the addresses are being processed in advance of the time when they are needed. The outputs of this multiplexer associated with the block code are "rotated" by RN in a  $1024 \times 5$  ROM programmed to perform the  $\oplus$  operation described in a later section. Finally, the addresses are clocked into another register which also complements each bit at the input of the inverting buss drivers. These drivers also implement the data save function by allowing MA to be held to all one's by the DATA SAVE switch on the power control panel during power turn-off. During  $\bar{R}$ , the EDXB, EDY signals from the DCU are selected to drive the MA buss through the same rotation ROM, register, and line drivers.

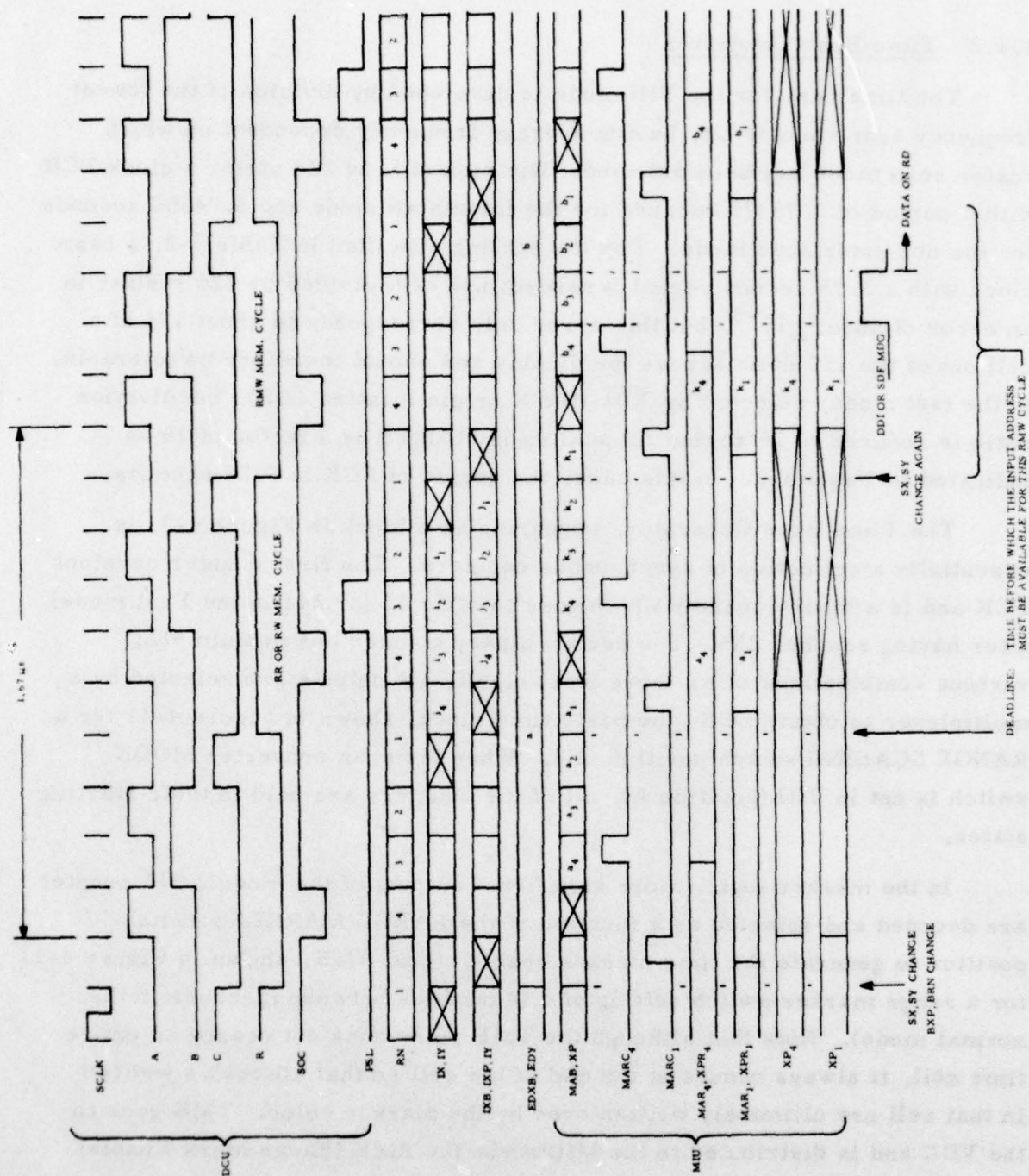


Figure 4-10. Memory Address Timing Diagram

#### 4.4.2 Time Base Generator

The time base for the THI mode is developed by division of the lowest frequency scan counter bit, having average frequency dependent on which raster scan mode has been selected. Division of L by 225 yields a clock FCK with a period of 3.75375 seconds for the interlaced mode and 3.74660 seconds for the non-interlaced mode. For the scaling specified in Table 3-2, a basic clock with a 3.75 second period is needed; use of L divided by 225 results in an error of about  $\pm 10^{-3}$ , but this error only corresponds to about 1/4 of a cell out of the 250 cells across the display and should therefore be tolerable. In the fast mode, selected by  $\overline{XUI}$  (the X origin location LSB), the division ratio is reduced to 15 so that all scaling is changed by a factor of 15 as indicated in Table 3-2. In this case, the period of FCK is 0.25 seconds.

The Time Base Generator, appearing as a block in Figure 4-9, is essentially a collection of synchronous counters. The first counter develops FCK and is a binary counter which goes to state 31 (or 241 in the Fast mode) after having reached 255. The second binary counter has modulo 512; various combinations of its three least significant outputs are selected by a multiplexer to obtain BCK, the basic time clock, shown in Figure 4-11 for a RANGE SCALING switch position of 4. When the scan converter MODE switch is not in THI (position A), all of the counters are held in their starting states.

In the marker logic, more significant outputs of the modulo 512 counter are decoded and selected as a function of the RANGE MARKERS switch position to generate the time marker enable signal TME, shown in Figure 4-11 for a range marker switch setting of 4 (4 minutes between markers in the normal mode). Note that although the TME pulse does not occupy an entire time cell, it always occurs at the end of the cell so that all colors written in that cell are ultimately written over by the marker color. TME goes to the VDU and is distributed to the MIU's via the RME (Range Mark Enable) lines.

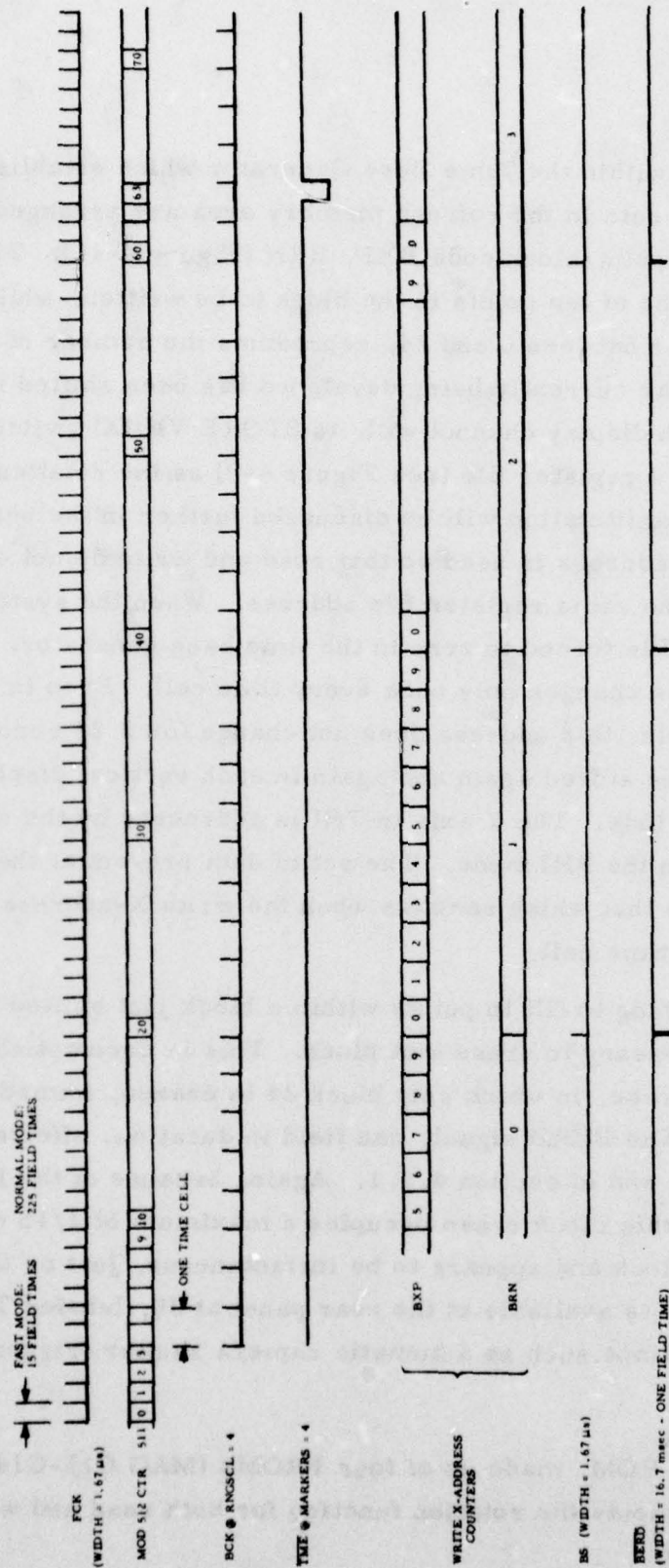


Figure 4-11. Time Base Generator Timing Diagram

The counters within the Time Base Generator which establish the X address for writing data in the refresh memory area are arranged to count in the special 9-bit point/block code BXP, BRN (Figure 4-11). The 4-bit code BXP selects one of ten points in the block to be written, while the 5-bit code BRN, a number between 0 and 24, represents the number of blocks by which the THI display currently being developed has been shifted left (see 3.1.3.1). For each display channel with its STORE VIDEO switch on, BRN is stored in the 5 x 4 register file (see Figure 4-9) as the rotation number  $RN_K$  for that channel (Rotation will be discussed further in the next section). The complemented address is used so that read and write do not occur simultaneously at the same register file address. When the system is not in the THI mode, BRN is forced to zero in the time base generator. In THI, the write X-address changes only once every time cell. Even in the fastest time scaling possible, this address does not change for 0.25 seconds, thus permitting data to be stored again and again in each vertical display column for many radar periods. The Y axis in THI is addressed by the coordinate converter just as in the RHI mode. The set of data present at the very end of each time cell is that which remains when the write X-address is incremented to the next time cell.

Before beginning to fill in points within a block just shifted into display block 24, it is necessary to erase that block. This is accomplished by initiating a block erase, in which only block 24 is erased, immediately after each block shift. The BERD signal, one field in duration, effects this erasure as described at the end of section 4.3.1. Again, because of the long duration of each time cell, this block erase occupies a maximum of 1/15 of the first time cell in each block and appears to be instantaneous, just as the normal erase does. BERD is available at the rear panel at J9, labeled THI BLOCK SHIFT, for applications such as automatic camera shutter triggering.

#### 4.4.3 Rotation

The 1024 x 5 ROM, made up of four PROMs (MAG C11-C14 in Appendix B) implements the rotation function for both read and write X memory addresses:

$$\begin{aligned}
 XB \boxplus RN_K &= XB \oplus RN_K; \quad XB < 25 \text{ (display area, Figure 4-8)} \\
 &= XB \quad ; \quad 25 \leq XB \text{ (ancillary data area, Figure 4-8).} \\
 &\quad \quad \quad \text{modulo 25}
 \end{aligned}$$

where  $XB$  is the block number (see Figure 4-8) and  $RN_K$  is the rotation number for channel  $K$ . During each time slot (see Figure 4-10), a different rotation number  $RN_K$  appears on  $RN$ , having been read from the  $5 \times 4$  register file addressed by  $A$  and  $B$ . For example, displays 1 and 2 might contain RHI's so that  $RN_1 = RN_2 = 0$ ; display channel 3 might hold a THI which has undergone 17 block shifts, hence  $RN_3 = 17$ ; while display 4 might be occupied by a THI which had been stopped earlier with  $RN_4 = 9$ . The  $RN_K$  are five-bit numbers, each ranging from 0 to 24. They rotate their respective displays only in the display area as described quantitatively above. This rotation is required to implement the "block shift" needed for the THI data entry scheme described in section 3.1.3.1.

Because the rotation does not include the ancillary data area, the ancillary data entry operation is not affected. The erase operations are not affected by the rotation since all blocks are covered and the order makes no difference. The DDI operations involving the cursor and slow read are with respect to the non-rotated scan, although the data obtained from the memory are from the rotated address. Thus, the cursor does not move as the THI display rotates under it and the color data obtained by a cursor data entry corresponds to what is displayed under the cursor.

During  $\bar{R}$ , an address from one of three sources, as selected by priority logic for each channel, appears on the MA and XP busses during the time slot reserved for that channel. When the SDF or DDI is the source, the X-block address is rotated so that, for example, when a THI is transmitted, it does not appear additionally rotated in the remote display. If the STORE VIDEO switch for channel  $K$  is activated in THI, then the block number BRN from the time base generator is stored in the register file as  $RN_K$ . If the store switch for channel  $K$  is activated in any scan converter mode other than THI, then zero is stored in the register file as  $RN_K$ . Thus, THI displays can be retained while PPI, RHI, or CAPPI presentations are entered into other channels and vice versa.

When storing a THI in channel K,  $24 \oplus \text{BRN}$  appears on the MA buss. Thus, suppose  $\text{BRN} = 3$  (three "block shifts" have taken place), then the actual X block being addressed in the memory is  $24 \oplus 3 = 2$ . Meanwhile,  $\text{RN}_K$  has been set to BRN so that the data appearing in the block 0 position on display K are from memory block  $\text{DXB} \oplus \text{RN}_K = 0 \oplus 3 = 3$ , those in block 1 are from memory block 4, 22 from 0, 23 from 1, and display block 24 is from memory block 2, which is where the writing is going on. Meanwhile, the XP buss is driven by BXP from the time base generator and the rest of the memory address, which corresponds to Y on the display, comes from the scan converter which is doing an RHI with any elevation angle. The resulting THI data entry is as described in section 3.1.3.1.

#### 4.5 Memory Interface Units

The block diagram in Figure 2-1 contains four Memory Interface Units (MIU) which are identical rack-mounted drawers. Address, clock, and gate busses are supplied to the MIU in a daisy-chain configuration where each unit taps off a twisted-pair cable which is resistively terminated only at the last MIU (No. 1). A block diagram of one MIU is presented in Figure 4-12; the detailed descriptions of various components within it are contained in paragraphs following a discussion of memory cycles.

##### 4.5.1 Memory Cycles

The timing diagram in Figure 4-13 shows all significant waveforms for examples of the four types of memory cycles. Each cycle occupies one-half period of the square wave R (shown in both timing diagrams, Figure 4-8 and 4-13), and is initiated by manual or automatic commands listed in Table 4-1. The state of R determines whether the raster-scan address DXB, DY or the code-converted input address IXB, IYB appears on the memory address buss.

As listed in the table, each of the four types of cycles happens in response to commands when the raster scan address DXB, DY is in certain areas of the display.



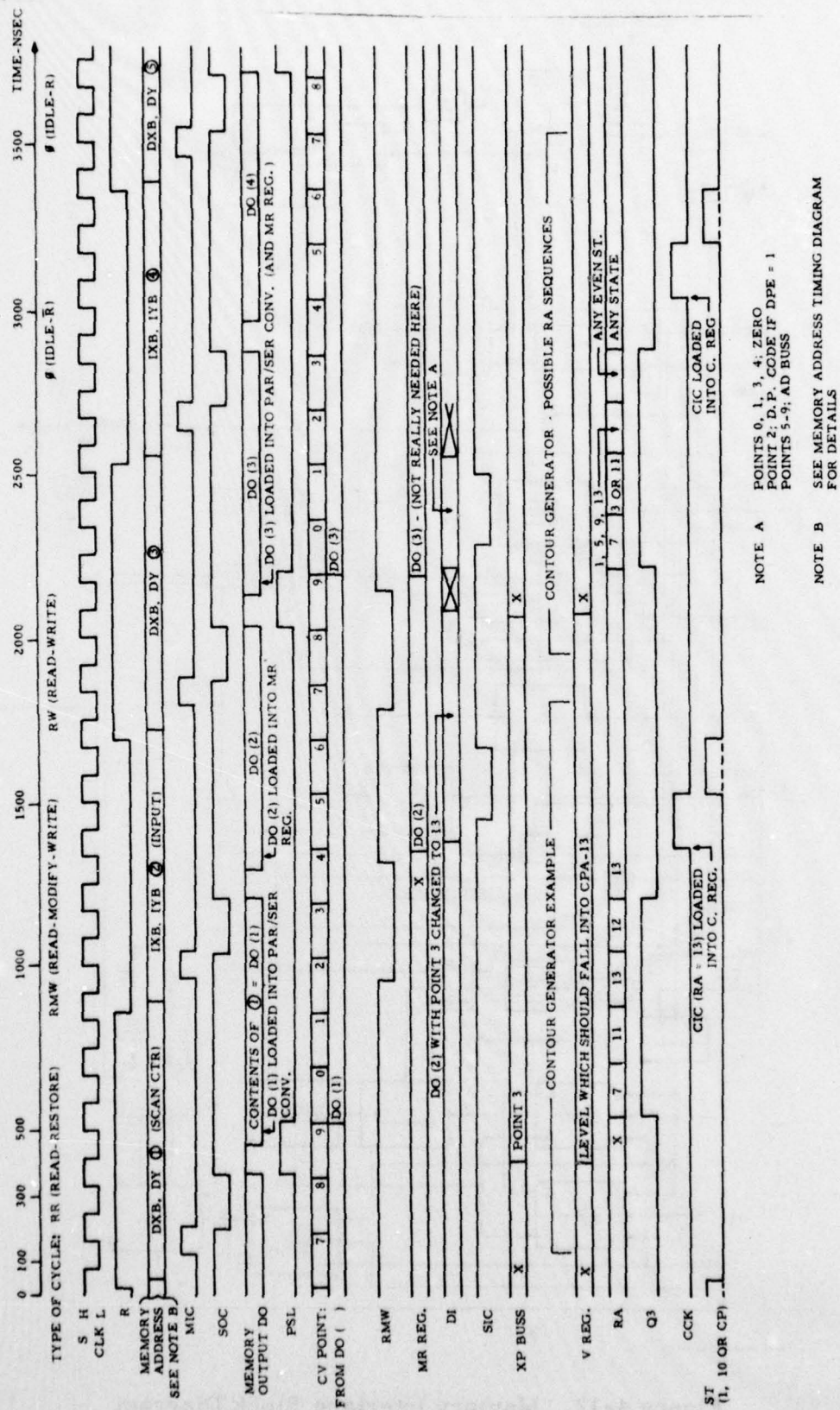


Figure 4-13. Memory Interface Timing Diagram

Table 4-1. Memory Cycles

<u>R</u>	<u>Commands</u>					<u>Type of Memory Cycle When DXB, DY is in each Area of Display(see Fig. 4-8):</u>			
	<u>Video Store</u>	<u>Legend Store</u>	<u>Erase</u>	<u>Parameter Store</u>	<u>Memory Address Buss</u>	<u>DA</u>	<u>LA</u>	<u>PA</u>	<u>Retrace</u>
1	X	O	X	X	DXB, DY	RR	RR	RR	Ø
1	X	1	X	X	"	RR	RW	RR	Ø
1	X	X	O	X	"	RR	RR	RR	Ø
1	X	X	1	X	"	RW	RR	RW	Ø
1	X	X	X	O	"	RR	RR	RR	Ø
1	X	X	X	1	"	RR	RR	RW	Ø
O	O	X	X	X	IXB, IYB	RR	RR	RR	RR
O	1	X	X	X	IXB, IYB	RMW	RMW	RMW	RMW

Listing of Types of Memory Cycles (see Figures 4-12 and 4-13)

<u>R</u>	<u>Cycle</u>	<u>Description</u>
1	RR	READ-RESTORE. Data from memory address DXB, DY are transferred to the parallel/serial converter and are available to the DDR multiplexer. Unchanged data are restored at the same address. This cycle is used for providing video information to refresh the raster-scan display.
1 or O	Ø	IDLE. Do nothing.
1	RW	READ-WRITE. Data from memory address DXB, DY are transferred to the parallel/serial converter and are available to the DDR multiplexer. New data, all zeroes for an erase operation or information from the AD (ancillary data) buss for legend or parameter storage, are written into the same address.
O	RMW	READ-MODIFY-WRITE. Data from memory address IXB, IYB are transferred to the modify/restore register and logic, then are partially changed and written back into the same address. This cycle is used to enter data into DA.

#### 4.5.2 Parallel-To-Serial Converter

Parallel data from the memory are loaded into this converter at a positive edge of SCLK during PSL--see the timing diagram in Figure 4-13. The converter is wired as a four-bit-wide, ten-bit shift register having a four-bit output CV which changes at positive transitions of SCLK. The timing diagram describes which point from which memory output appears at each time interval. The D MASK output (see Figure 4-12) is simply MASK, a signal which blacks out the undesired areas of the display, delayed by three SCLK periods so that it changes only at boundaries between points zero and nine.

#### 4.5.3 Color Encoder

The color encoder (see block diagram in Figure 4-14) accepts the four-bit output of the parallel-to-serial converter, and if DMASK is false, outputs three analog voltages to drive the red, green and blue video inputs on the color monitor. The three identical D/A converters only have three bits each, but nevertheless it is possible to generate 512 different color/intensity outputs. Voltages at each output take on eight different levels ranging from zero (black) to one volt (full intensity); the output loading must be 75 ohms through video coaxial cable.

The color encoder is programmable; that is, for each of the sixteen possible states of the input CV, an arbitrary set of analog output voltages can be programmed by means of switches. The switches are arranged in columns by colors, as shown in Figure 4-14, where an example of one possible program is shown. Within each column are three sub-columns which correspond to the bit weight 1, 2 or 4; finally, each switch in each sub-column is numbered from 0 to 15 to denote CPA (Color Patch Address--see Figure 4-8). In the example, the relative video values listed are obtained by simply adding the bit weights for each color at each CPA.

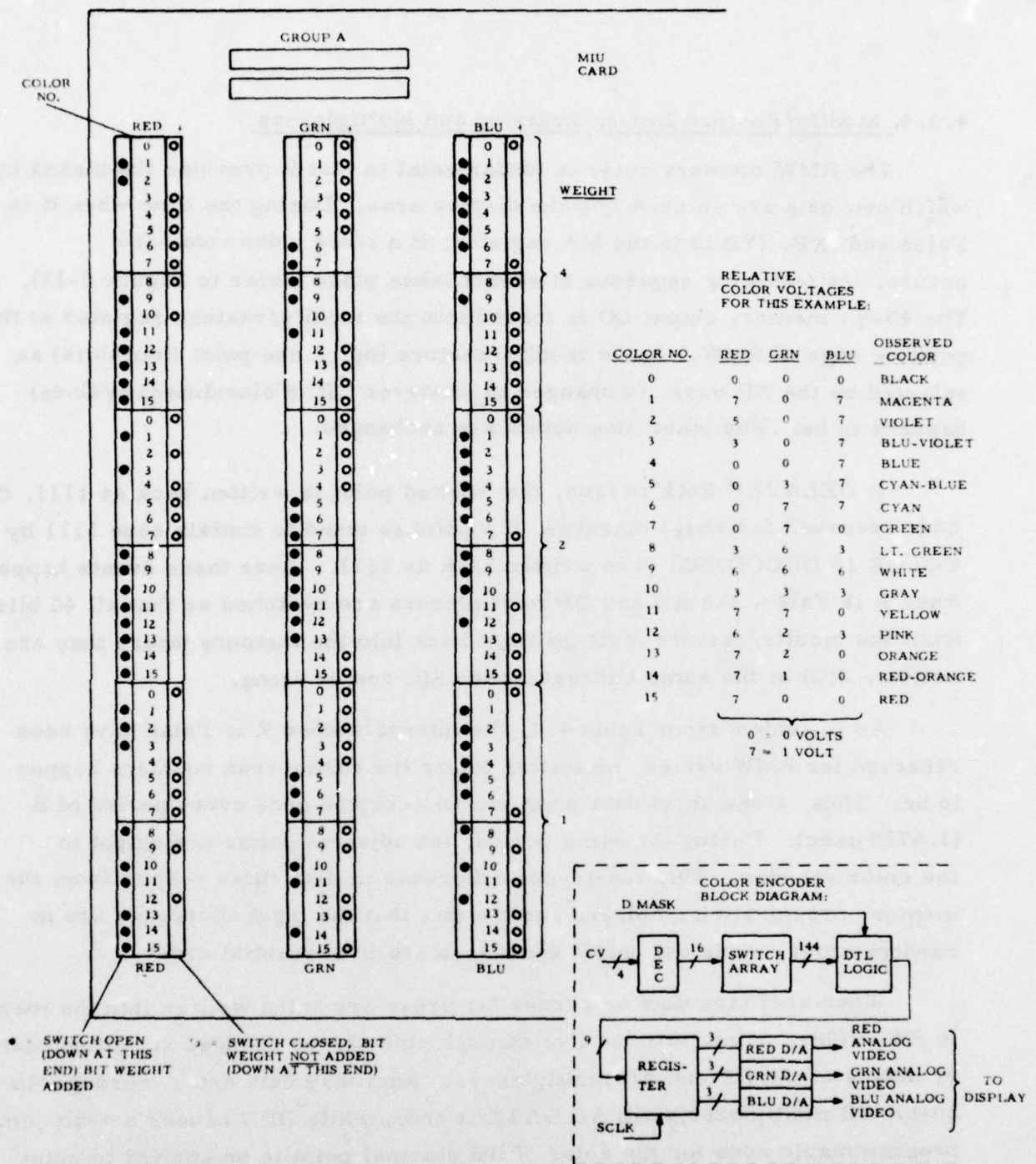


Figure 4-14. Color Encoder Switches and Block Diagram

#### 4.5.4 Modify/Restore Logic, Register and Multiplexers

The RMW memory cycle is fundamental in that it provides the means by which new data are entered into the display area. During the time when R is False and IXB, IYB is in the MA register, if a store video command occurs, the following sequence of events takes place (refer to Figure 4-12). The 40-bit memory output DO is loaded into the modify/restore register at the positive edge of RMW. In the modify/restore logic, one point (four-bits) as selected by the XP buss, is changed to whatever CIC (Color-Intensity Code) happens to be. The other nine points are unchanged.

If DELAYED RME is true, the selected point is written back as 1111, the code reserved for range markers. If a point is found to contain code 1111 by the COLOR 15 DECODERS, it is written back as 1111. Since these events happen when R is False, the AD and DP multiplexers are switched so that all 40 bits from the modify/restore logic go right back into the memory where they are written, still at the same address, when SIC comes along.

As is evident from Table 4-1, the intervals when R is False have been reserved for RMW cycles, no matter where the raster scan counters happen to be. Thus, a new input data point can be accepted once every period of R (1.6725  $\mu$ sec). During the same period, ten adjacent points are output to the color encoder. This ten-to-one difference in data rates results from the memory organization employed and the fact that the input addresses are in random order, while the output addresses are in sequential order.

When ancillary data or zeroes for erase are being written into the memory in RW cycles, points two and five through nine can be changed simultaneously by means of the DP and AD multiplexers. Ancillary data enter through the 20-bit AD multiplexer when AD GATE is true, while DPE causes a 4-bit jumper-programmable code for the color of the decimal point to be applied to point two. ZID zeroes all 40 bits during erase.

#### 4.5.5 Contour Generator

The lower half of Figure 4-12 is the contour generator which accepts one 8-bit video word and RME every period of R and presents a corresponding four-bit CIC (Color/Intensity Code) and delayed RME as its output. Contour thresholds, both colors and levels, are read from the memory when the raster scan is in the appropriate patch (see Figure 4-8) and are stored in register files -- small, fast memories capable of simultaneous reading and writing at different addresses. Data from the register files are used in a successive approximation algorithm to determine which CIC to assign to a given video input.

The incoming digital video is both scaled and converted to BCD in a ROM made up of two 256 x 4 PROMs, D9 and D10 for which truth tables are included in Appendix B. The ROM output is clocked by PSL into the V register where it remains available to drive the comparator during the remainder of the period of R. The example at the bottom of Figure 4-13 shows a digital video input which has a value such that it should be assigned the color which has been entered into CPA 13. The successive approximation register state RA always begins as seven whereupon the contents of the 1's and 10's register files at read address RA = 7 are compared with V. The decision made in the comparator determines that the next state for RA should be 11 (the other alternative is three), and the process continues to repeat in this manner until four decisions, corresponding to 16 bits, have been made. The final answer of RA = 13 then addresses the Color Patch Register File which provides a four-bit code to be loaded into the CIC register by CCK. The second contour generator cycle at the lower right of Figure 4-13 shows all possible states of RA for each step. Data sheets for the AMD 2503 successive approximation registers have been included in Appendix A.

The time interval after CCK is reserved for writing data into the three register files, as commanded by the three write strobe signals 1 ST, 10 ST and CPST. The write address applied to the register files is CPA, and the appropriate write strobe signal is gated-on when the raster scan is in the proper patch. Although each patch contains a five-by-four array of identically coded points, only one is needed to be written into the register files. Point

eight has been arbitrarily chosen and is thus loaded into the D register (Figure 4-12) at PSL so that it can be entered into the proper register file when the corresponding write strobe signal occurs. Four write strobes appear during each field for every write address of the register files.

#### 4.5.6 Memory Address Buss

In each Memory Interface Unit, the time-multiplexed MA and XP busses drive registers clocked by  $MARC_K$ , a pulse unique to time slot K for display channel K. Figure 4-10 illustrates the timing for channels 1 and 4; although they are clocked at different times, the registers in all four MIU's contain the proper addresses well in advance of SOC, during which they must be stable. The XP bits require an additional register clocked by the trailing edge of MIC (not shown on Figure 4-10 but coincident with the negative going edge of SOC) so that they can remain stationary during each RMW cycle. The  $MARC_K$  pulses are generated by breaking the chain of one twisted pair in the clock/gate buss and delaying the  $MAST_K$  clock by one period of SCLK on each MIU.

#### 4.5.7 Write Data and Read Data Busses

The WD and RD four-bit busses, daisy-chained through the MIU as are the other busses (see Figure 2-1), permit direct access to any image point in the memory for the SDF or DDI.

When the MWE control line is active, the multiplexer at the bottom of Figure 4-12 connects the WD buss directly to the CIC inputs of the Modify/Restore Logic. The Range Marker Enable signal is simultaneously rendered inoperative.

When the MDE control line is active, the tri-state driver at the top of Figure 4-12 drives the RD buss with a four-bit code corresponding to one of the ten points currently available at the memory output. The DDR multiplexer selects this point as a function of the state of the XP Buss. The RD buss differs from all others in that signals flow away from the MIU; more than one MDE control line cannot be active simultaneously lest the buss drivers perish.

#### 4.5.8 Cursor Interface

When the CUB (Cursor UnBlank) control signal is active, a cursor color code is applied to the CV inputs of the color encoder instead of the parallel/serial converter output. The color change logic ensures visibility of the cursor by defining its code as zero (black) except when the point being covered by the cursor (hence the background) is any of colors zero through three. In the latter case, the cursor appears as the jumper-programmed color, presently wired as color seven (light green).

The leading edge of the CDE (Cursor Data Enable) control signal enters the current four-bit word at the parallel/serial converter output into the cursor data register. As long as CDE remains active, this word appears on the RD buss. Individual MIUs are protected against simultaneous occurrence of MDE and CDE; CDE has priority.

#### 4.5.9 Full-Screen Operation

When the FSE (Full-Screen Enable) control line is active, the MASK which normally blanks certain areas among the ancillary data is inhibited. This condition permits use of the full screen for display of data written through the WD buss.

### 4.6 Serial Data Formatter/Video Distribution Unit

The SDF/VDU card contains two functional units which are only marginally interrelated. The VDU distributes video data and memory control signals from various sources to the MIUs. The SDF generates addresses to obtain, serially from the display memories, data which it synchronizes with an external clock and combines with synchronization codes for transmission to the RRM.

#### 4.6.1 Video Distribution Unit

The VDU card consists of an array of logic and line drivers which serves to distribute the eight-bit video signals from the coordinate converter to all of the MIUs. The memory control lines SIC, SOC, RMW, RME, and ZID for each MIU are also routed through the VDU, while the memory clock,  $\bar{R}$ , passes through on its way to the coordinate converter.

The video inputs for MULTIPLE DATA SOURCE (inputs on J12, J13 and J14) come directly to the VDU where, when MULTIPLE DATA SOURCE has been selected, they are synchronized with the appropriate memory timing signals and coordinate-converter-generated memory addresses for distribution to the assigned display refresh memory. The synchronizer circuitry is of the same design as that described in section 4.2.8. When MULTIPLE DATA SOURCE has not been selected, the video input on J1 is routed to all display refresh memories.

#### 4.6.2 Serial Data Formatter

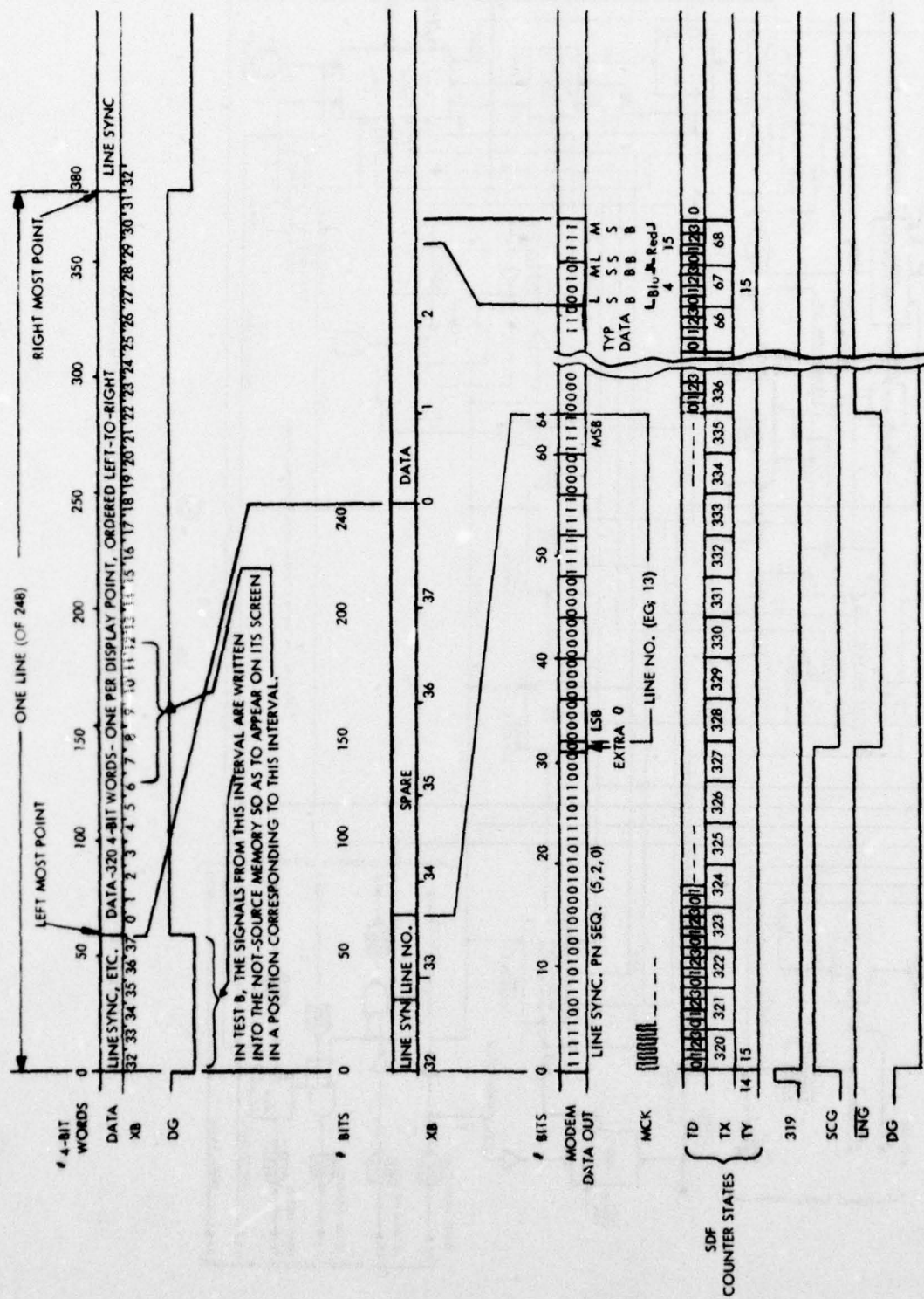
A multiplexer, illustrated in the upper left corner of Figure 4-15, selects the X and Y coordinate converter outputs for application to the DDI address inputs TSX, TSY when TASM from the MAG is low. A decoder detects  $SX = 255$  so that the DCU can disable the store commands in this case since radar data must not appear in the ancillary data area which begins at  $X = 255$  (see Figure 4-8). When TASM is high, the DDI address inputs are driven by the transmit address counters TX and TY.

The serial data format appears in Figure 4-16 along with certain SDF waveforms included to show the operation of the counters in Figure 4-15. The counters are synchronous with the clock MCK which, with the TEST CLOCK switch off, comes from the MODEM transmit data clock converted to TTL levels. Interface with the memory, having faster clocks SCLK and PSL, is affected by separate read and write synchronizers.

The bit counter operates differently between the transmit and test modes, but its least significant two bits TD always define the bit number (0-3) of the point specified by the transmit point and line counters TX, TY.

In the transmit mode (see Figure 4-17) the counter has modulo four and the write synchronizer is disabled. Consider the time when TX has just changed from  $X_1 - 1$  to  $X_1$  in Figure 4-17. The expanded-time-scale waveforms show how the read synchronizer subsequently generates an MDG pulse at the earliest possible time consistent with the memory timing. Recall that MDE is the control line which activates a tri-state RD-buss





**Figure 4-16. Serial Data Format**



Figure 4-17. Transmit Mode Timing

driver in an MIU. MDG is simply applied to the MDE line for whichever MIU has been selected as the source by the DISPLAY switch which drives the Test/Select logic (see Figure 4-15). While MDG is active, the four-bit color/intensity code obtained from the memory address defined by  $X_1$ , Y (the present states of counters TX, TY) is on the RD buss. At the trailing edge of MDG, this word is clocked into a register and becomes SRD, the read synchronizer data output. SRD is serialized by a multiplexer, enabled only during the data gate DG (Figure 4-16), with its select inputs driven by TD. The resulting serial data is or'd with serial sync. code and line number signals, each gated on during its appropriate time, and the entire serial data stream is re-clocked by MCK to become MD which drives the Modem through a multiplexer and line driver which level-converts to the EIA Standard RS 232 interface signal levels.

The preceding paragraph also applies when either test mode is selected, except that the Modem Data Output is disabled and the bit counter has modulo eight. The WIG signal shown in Figure 4-18 initiates a write operation in which a four-bit word, having been obtained from the source memory and serialized as described above, is shifted into a parallel output register which drives the WD buss. This four-bit word is subsequently written into another memory at the same address, since TX and TY haven't changed yet. The expanded-time-scale waveforms of Figure 4-18 show how MWG is developed from the WI pulse by the write synchronizer. The test/select logic (Figure 4-15) directs MWG to the MWE inputs of the DCU and the MIU with channel number one greater than that selected as the source. The normal store command inputs of the DCU are not used in this mode.

Test Mode A causes the source memory to be copied into another memory, while test mode B results in waveforms from the time when DG is False (Figure 4-16) being written into another memory. Test Mode B thus requires that the WI pulse be active only when DG is false and that the X address be scrambled (TX8 complemented) when WIG is true.

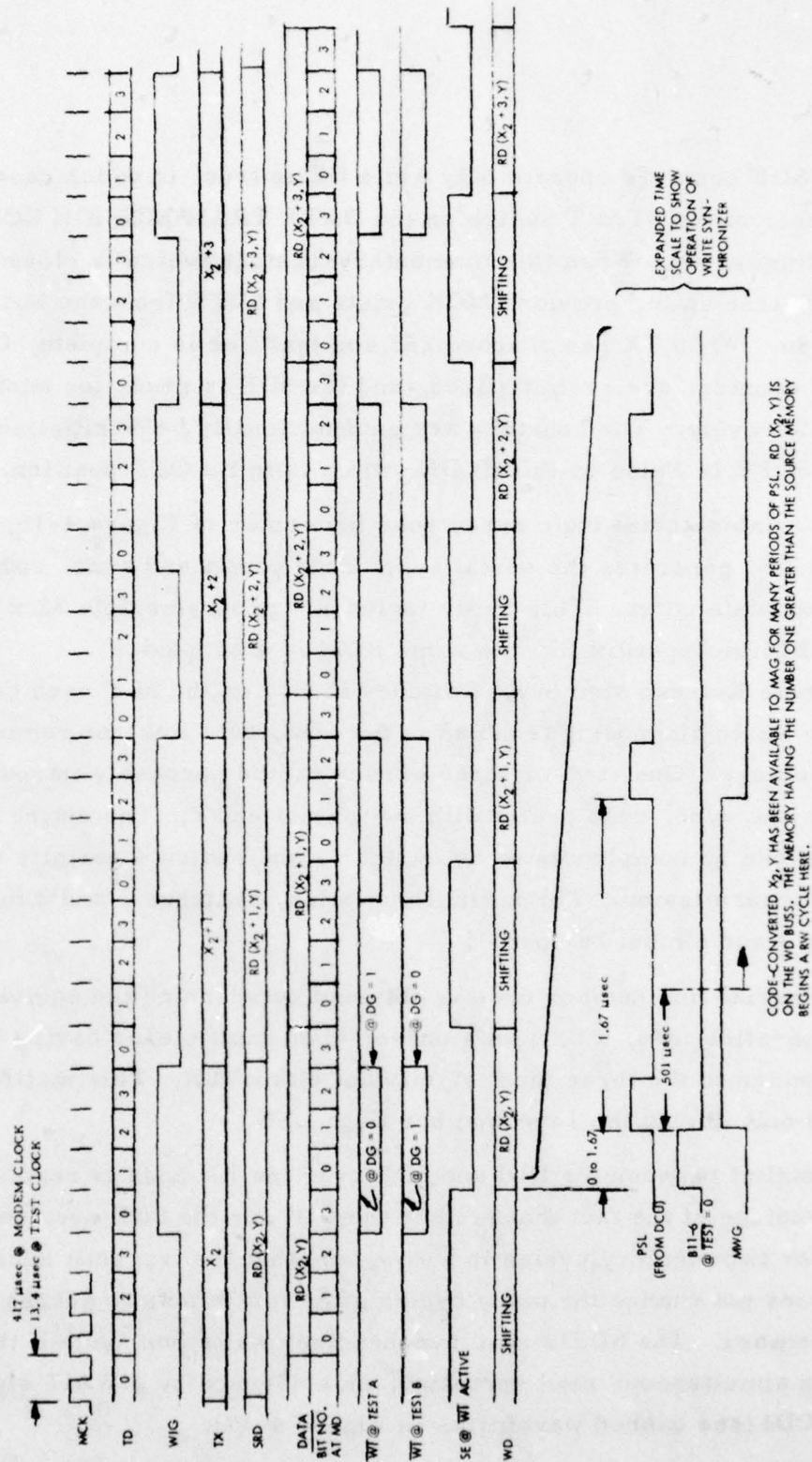


Figure 4-18. Test Mode Timing

The SDF counters operate only while CE is true, in which case the blue indicator of the START switch on the DATA TRANSMISSION CONTROL Panel is illuminated. When this momentary-contact switch is closed, CE is set to its true state, provided MCK exists and SDFE from the MAG priority logic is true. When TY has reached 253 and that line is complete, CE is reset, the counters are re-initialized, and the SDF is ready for another transmission cycle. The counters are unconditionally held initialized whenever SDFE is False or the MODE switch is in its OFF position.

The combinatorial logic array near the center of Figure 4-15, driven by TD and TX, generates the serial sync. code prefix and sync. code, line number, and data gates. This array includes a programmable 32 x 8 ROM (see SDF B15 in Appendix B); the same ROM is also used in the Remote Refresh Memory. Switches in B30 on the SDF card can be used as an aid in diagnosing troubles in the SDF, data link, or remote refresh memory. One, two or three errors can be purposely introduced into every line sync. code prefix with switches 1 and 2. The entire line sync. code can be complemented by switch 3, and switch 4 permits continuous, repetitive transmission. For normal operation, switches 1 and 2 must be closed and 3 and 4 must be open.

The serial line number code is obtained by scanning the equivalent eight-bit parallel code, TY, with a one-of-eight multiplexer having select lines connected to the three least significant bits of TX. This multiplexer is enabled only during the Line Number Gate LNG.

A conflict between the DDI and SDF over the RD buss is resolved by taking advantage of the fact that neither the DDI nor the SDF ever needs the RD buss for two memory cycles in a row, and that the transmit address in the SDF does not change for many cycles after it attempts to access the display memory. The SDF's read synchronizer waits one cycle if the DDI attempts a simultaneous read operation, as evidenced by a WAIT signal from the DDI (see dashed waveforms in Figure 4-17).

The array of logic and level interface elements at the lower left of Figure 4-15 provide for interaction between the MODEM, the CRT terminal, and the SDF. The SDF has priority over the outbound direction of data transmission through the MODEM; during a data transmission, the Master CRT terminal cannot transmit to the Remote one. Communication in the other direction, however, is always possible.

#### 4.7 Display Data Interface

The Display Data Interface (DDI) includes a multitude of interfaces necessary so that the DISPLAY INTERFACE CONTROL Panel, DCU, MIU, SDF, and the computer's Universal Logic Interface (ULI) can collectively communicate. These interfaces include A/D conversion of the trackball outputs, code-conversion, generation of precisely-timed control signals, temporary storage of data, routing of data, synchronization, and sequential control of data transfer operations. Reference to the DDI Block Diagram in Figure 4-19, unless otherwise specified, is implied in the following sections.

##### 4.7.1 Cursor Position

Digital binary-coded representation of cursor position (XC, YC) is derived from a mechanical trackball device (see Appendix A) on the LWCA control panel. Bipolar voltages, obtained by zener regulation from the 15-volt supplies, are applied across the 10K trackball potentiometers. The resultant bipolar analog signals--one proportional to X-axis (left-right) displacement, the other to Y-axis displacement--are low-pass filtered and converted to binary-coded digital form in Datel ADC MA-10B modules (see Appendix A).

The converter modules are set up so that an input voltage of -10 volts gives an all zeroes output, while +9.9951 volts yields all ones. Outside of this range, the converters limit. The Y-channel analog voltage range is  $\pm 12$  volts (the last two volts at either end is not used) and the most significant eight bits of the converter output are clocked into a register to become YC.

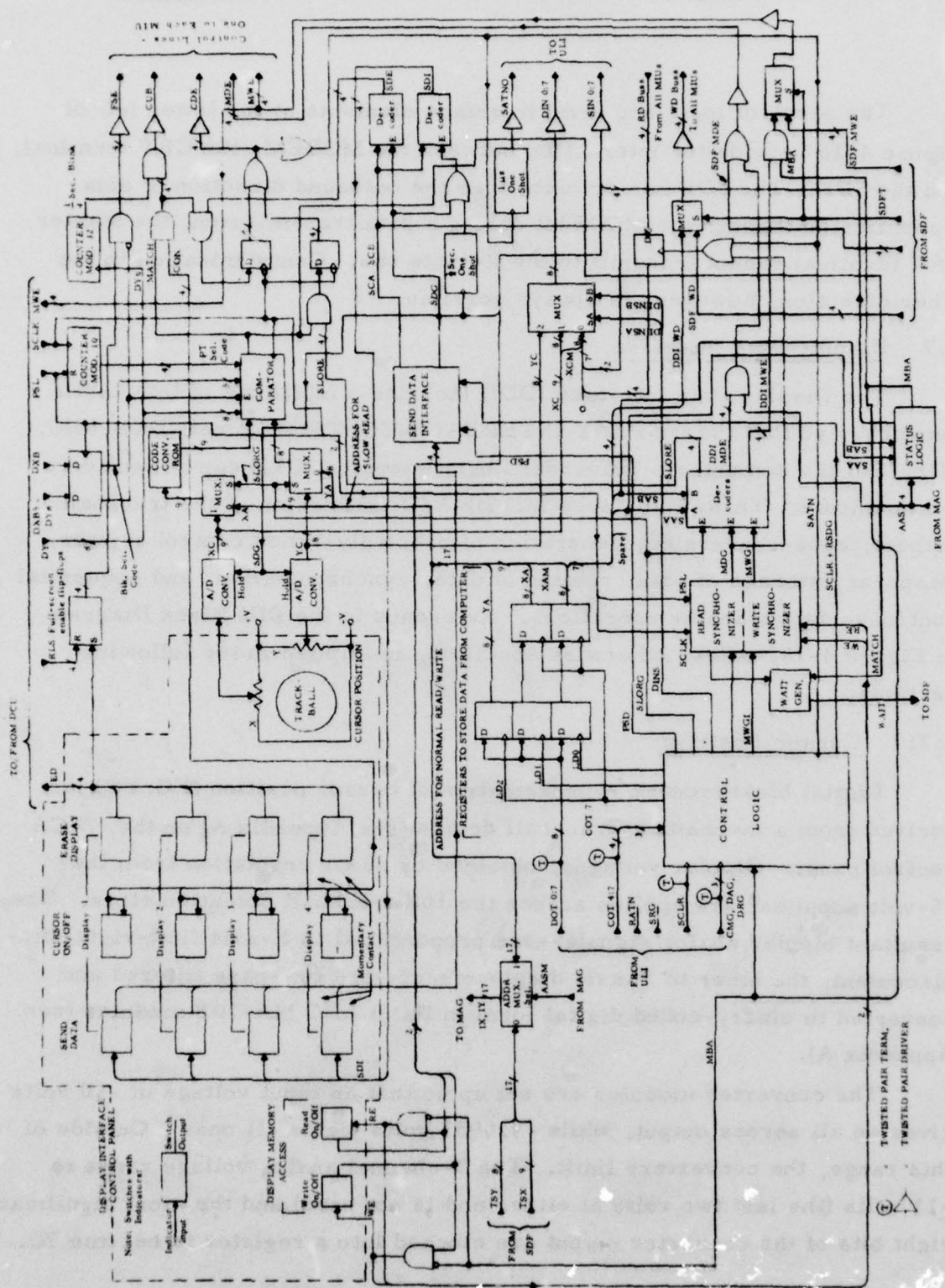


Figure 4-19. DDI Block Diagram

The X-channel analog voltage range has been limited by a series resistor to -12 to +3.4 volts, while the most significant nine bits of its converter output are clocked into a register to become XC. Although the X analog voltage is limited, it is possible to exceed  $XC = 319$ , which is beyond the right edge of the screen. This condition is discussed from an operational standpoint in section 3.1.10.

In order to remain compatible with Interdata notation, YC and the least-significant eight bits of XC are numbered with the most significant bit having the least subscript--just opposite to all other scan-converter documentation. The MSB of X is handled separately as XCM; for an illustration of display addressing convention, see Figure 2 of AJJ-21 in Appendix C.

The self-clocked, successive-approximation A/D converters begin a conversion once per raster-scan field, at the trailing edge of DY7. Conversion is inhibited when SDG, the send-data gate to be discussed later, is true. This feature prevents (XC, YC) from changing during a data transaction.

#### 4.7.2 Cursor Generation

The cursor, a moveable single point on the screen, is made to appear by the generation of a narrow pulse properly timed with respect to the raster scan. This pulse is applied to the CUB input (described in section 4.5.8) of each MIU having its CURSOR ON/OFF switch in the on (illuminated) state.

Except for the Slow-Read case to be described later, XC and YC pass through the digital multiplexers shown. The code conversion ROM develops the special block/point code used in the DCU and MAG for generating X addresses, so that a digital comparison can be made directly. The raster scan location is defined to the nearest 10-point block by DY and DXB from the DCU. The state of the mod-10 counter driven by SCLK and reset by PSL defines the location of a point within that block. When the

scan location equals the cursor location, the comparator MATCH output becomes true and the logic shown generates a CUB (cursor unblank) for those displays having their cursor switched on. The cursor is made to blink with a 0.5 second period in order to make it easy to find and to see what color it covers. The blinking can be disabled by closing switch 1 on C26 of the DDI. The comparator is disabled when the DXB5 + DY8 signal, corresponding to the vertical and horizontal blanking intervals, is true.

#### 4.7.3 Full-Screen Enable

The flip-flops which are set by the ERASE DISPLAY buttons and reset by signals RLS (from the DCU and the STORE THRESHOLD buttons), simply generate the FSE (full-screen enable) signals. When FSE is true for a given display, the mask which normally surrounds the color patches and alphanumeric characters is disabled so that the full screen can be used. FSE is inhibited during retrace time intervals.

#### 4.7.4 Address Multiplexer

The multiplexer at the center-left of the DDI block diagram selects whether the MAG inputs are to be driven from the SDF outputs as they normally are, or from the computer. It selects the X and Y SDF outputs TSX, TSY for application to the MAG address inputs IX, IY when AASM from the MAG is low, or the outputs of temporary data storage registers YA, XA and XAM, when AASM is high.

#### 4.7.5 DISPLAY MEMORY ACCESS Controls

The logic shown connected to the READ ON/OFF and WRITE ON/OFF switches and indicators disables these operations if MBA (Memory Buss Available) is False. MBA, developed in the status logic, is true only if

1. Neither SDF TEST mode has been selected,
2. The channel most recently addressed by the computer (SAA, SAB) is not involved in a higher-priority operation.

Status bits, available to the computer, indicate which channels are useable as shown in Table 4-2.

Table 4-2.								
DDI (Device X '8B') Status Byte (Different from LWCA DDI)								
Bit:	<u>0</u>	<u>1</u>	<u>2</u>	<u>3</u>	<u>4</u>	<u>5</u>	<u>6</u>	<u>7</u>
True (Logic 1)	Display Channel	Display Channel	Display Channel	Display Channel	SDG	WRITE Switch	READ Switch	SPARE
Condition:	1 Not Available	2 Not Available	3 Not Available	4 Not Available		ON	ON	
All true if SDF TEST A or B selected.								

Examination of the status bits by the computer is entirely passive and does not affect DDI operation in any way. Bits 5 and 6, from the DISPLAY MEMORY ACCESS switches also control operation of the Read and Write synchronizers.

#### 4.7.6 Computer Interface

The Interdata M48-013 Universal Logic Interface, described in their publication number 29-311, is a circuit card located within the computer itself. Line drivers and receivers for the signals indicated as "from ULI" and "to ULI" in the DDI block diagram have been built onto the ULI. The signals reach the DDI through a multiple twisted-pair cable having connectors at the computer's convenience panel.

The ULI is always operated in its Byte Mode. Data arriving at the DDI from the ULI on DOT 0:7 are loaded into one of three registers, according to load commands LD0, LD1 and LD2 from the control logic. Three of the user defineable command bits COT 4:6 and most of the control lines are used to drive the control logic, causing it to change state (as the computer executes I/O instructions with device number X'8B') according to the diagram in Figure 4 of AJJ-21 in Appendix C. The control logic is implemented as a four-bit sequential machine with two field-programmable 32 x 8 ROMs (see Appendix B-DDI B23, B29 ) in its feed-back path. These ROMs have been programmed to cause the control logic to behave as characterized in the state diagram. A different section of one ROM can be selected to alter the behavior of the control logic for hardware tests covered in a later section.

The Read and Write synchronizers match the timing of certain control logic outputs to that of the scan converter. Control logic outputs are directed to the proper display channel by the decoders shown driven by the two-bit display select code SA received in one of the registers. Of these outputs, DDI-MDE and DDI-MWE drive the MIU circuitry through logic which combines them with their counterparts from the SDF, while the SLORE (Slow Read Enable) signals permit generation of corresponding CDE (Cursor Data Enable) control pulses following a subsequent MATCH occurrence. CDE pulses can also be generated similarly following a manually initiated send-data sequence. The incidence of any CDE results in the following actions: 1) A one-microsecond pulse is sent to the ULI on its SATNO (interrupt input) line, 2) the 4-bit word now on the RD Buss is stored in a register accessible to the ULI, and 3) the control logic state changes. Control logic, synchronizer, and CDE operation are exemplified in the next section where specific types of data transfers are explained.

When a possible conflict with the SDF over the RD buss is impending, either because of a MATCH occurrence at certain critical times (with the possibility of a subsequent CDE) or because of a memory read operation being handled by the DDI Read Synchronizer, the Wait Generator outputs a pulse to the SDF Read Synchronizer.

A multiplexer, driven by DINS (Data Input Select) from the control logic, selects data from various points in the DDI to be sent over DIN 0:7 to the ULI.

#### 4.7.7 Data Transfers

The explanations of the various types of data transfers, contained in the following sub-sections and supported by detailed timing diagrams, parallel those appearing in AJJ-21 of Appendix C. Because the same examples have been used, correlation between the software-oriented information in AJJ-21 and the hardware-oriented discussions to follow should provide a thorough understanding of this interface. Note, however, that AJJ-21 was written for the LWCA system and therefore has a different status byte along with other differences because the associated scan converter does not have a time-multiplexed memory buss. The section titled "Operation of the LWCA Scan Converter" should be ignored.

#### 4.7.7.1 Write Display Memory

The three different types of write operations are each represented in Examples 1, 2 and 3 of Figure 4-20. The leading edge of the first CMG pulse, occurring in response to execution of an OC instruction as indicated in the corresponding software example, coincides with the appearance of the code 000 on ULI outputs COT 4 through 6. The trailing edge of CMG compels the control logic to enter state RW1.

New data (not shown) appear on ULI outputs DOT 0 through 7 at the leading edge of each DAG pulse, while the control logic changes state at each trailing edge. The mutually-exclusive Load commands LD0, LD1 and LD2 occur during each DAG pulse in states RW1, RW2 and RW3, respectively. The trailing edge of each LD pulse loads the then-stable ULI data outputs into the appropriate register. The data do not all reach their final registers, however, until the last transition of LD2. The extra registers were added so that all 17 memory address bits change simultaneously; thus, avoiding possibility of anomolous behavior in certain situations.

As the control logic leaves state RW3, the Write synchronizer springs into action, driven by MWGI. If WE is true (write indicator lit), the synchronizer generates an MWG (Memory Write Gate) pulse starting at the next positive edge of the PSL clock (from the DCU) at least 400 nanoseconds after the control logic state transition. At this time, all address bits are in their proper registers, the four-bit color/intensity code to be written is in a register driving the WD buss, and the display select code is at the decoder select inputs so it can direct the MWG pulse onto the proper MWE line. The write operation for one point is thus completed during the MWG pulse. Had WE been false (write indicator not lit), no MWG would have been issued.

The three examples in Figure 4-20 differ only in the path taken through the control logic states, as determined by COT 4:6 (of the command byte). They each involve writing two points which could be accomplished as in example 3, but in examples 1 and 2, advantage has been taken of common information between the points or compact table organization to shorten the total execution time.



#### 4.7.7.2 Read Display Memory

The write data transfer just described can be executed only if the scan converter memory buss\* is available. The normal read display memory operation, example 4 in Figure 4-21, also requires the memory buss. A slow read transfer, example 5 in the same figure, does not need the buss but requires an interrupt service routine in the software and may occupy a lengthy time interval.

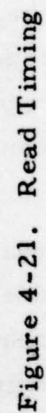
Through state RW3, the normal read sequence is the same as a write sequence, except that a different command byte is issued. When the control logic goes from state RW3 to R4, the read synchronizer begins its work. Depending on the current phase relationship between the scan converter and the computer, the MDG pulse ends 1.5 to 3.17 microseconds after the state transition. At this time, the color-intensity code for the addressed point which had been on the RD buss during MDG, is clocked into a register on the DDI. Because DINS = 0, the outputs of this register reach ULI data inputs DIN 4:7. Note that on the DDI schematic, the inputs and outputs are oppositely numbered; this is another case where the Interdata bit-numbering convention conflicts with that established for the scan converter.

Because up to three microseconds can elapse before the data are ready, a delay should be programmed so that the DRG pulse from the MIU does not happen too early. This DRG pulse, the result of execution of a read instruction--see the corresponding software example--transfers the signals at the ULI data inputs to the computer and sends the control logic back to state RW1. Another point can now be read, or as in the example, a CMG pulse with command byte 010X111X issued to force the control logic into state I.

Should the memory buss\* not be available (MBA = false), the slow-read sequence (example 5 in Figure 4-21) must be employed to obtain data from the image memories. This sequence, through state RW3, is identical to that of a normal read. Command bit COT 6 can be left as a zero since the fact that MBA is false will force the control logic to follow the proper state sequence, or it can be set to a one in which case the slow read will be performed even if MBA is true.

---

\* for the selected display channel.



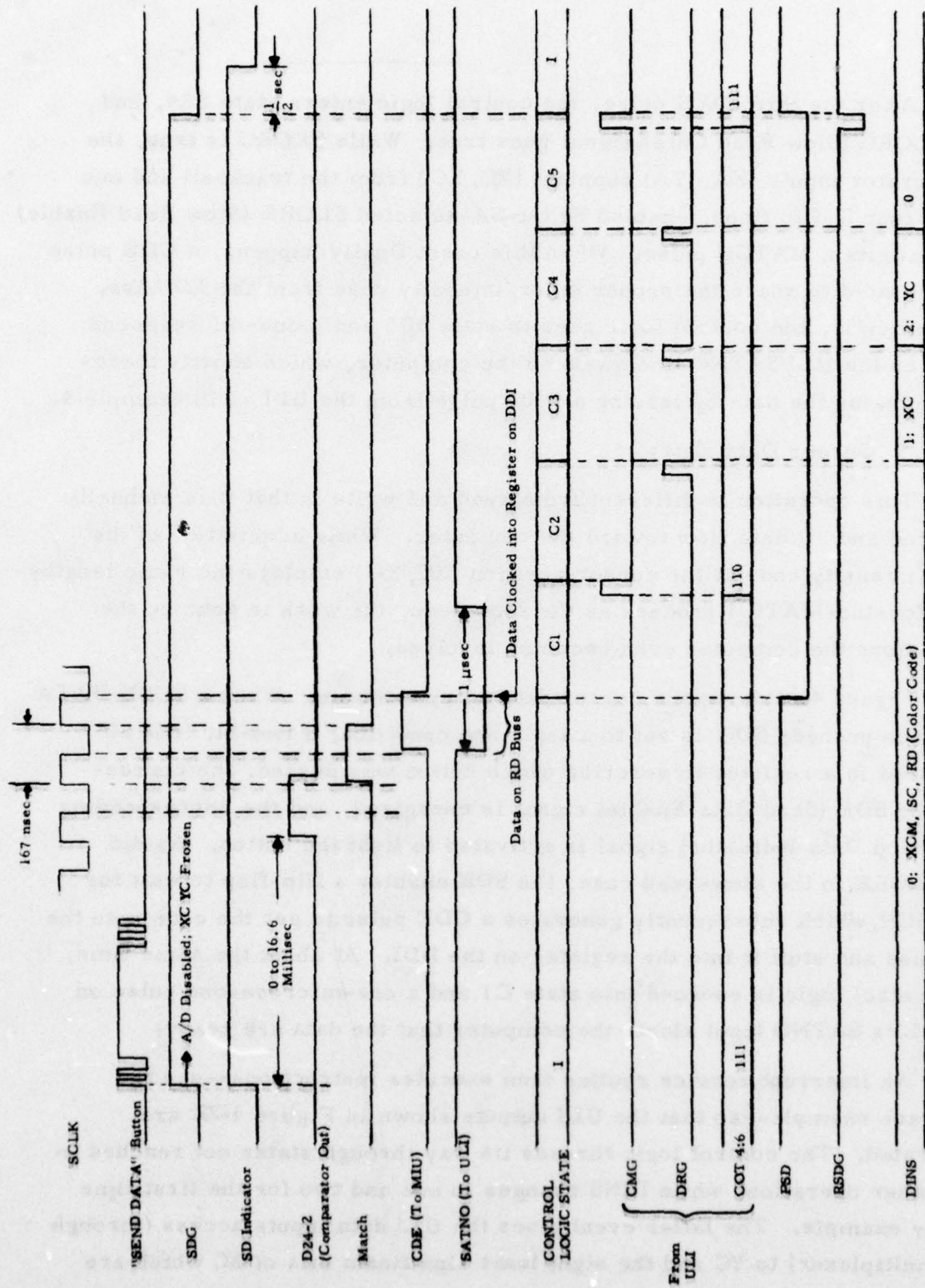
After the third DAG pulse, the control logic enters state SR4, and the SLORG (Slow Read Gate) signal goes true. While SLORG is true, the comparator inputs (XA, YA) supplant (XC, YC) from the trackball and one of the four D-flip flops, enabled by the SA-selected SLORE (Slow Read Enable) line, awaits a MATCH pulse. When this event finally happens, a CDE pulse is generated to snare the proper color/intensity code from the RD buss. Concurrently, the control logic goes to state SR5 and a one-microsecond pulse on the ULI/SATNO line awakens the computer, which shortly thereafter obtains the data by issuing a DRG pulse from the ULI as in example 4.

#### 4.7.7.3 Cursor Data Entry

This operation is different from read and write in that it is manually initiated and all data flow toward the computer. While acquisition of the color/intensity code at the cursor position (XC, YC) employs the same lengthy wait-for-the-MATCH process as the slow read, the work is done by the DDI before the computer even becomes involved.

Figure 4-22 shows the cursor data entry example. When a SEND DATA button is pushed; SDG is set to a logic one condition, a two-bit code SC is stored in a register to describe which button was pushed, the corresponding SDE (Send Data Enable) signal is energized, and the corresponding SDI (Send Data Indicator) signal is activated to light the button. As did the SLORE in the slow-read case, the SDE enables a flip-flop to wait for a MATCH, which subsequently generates a CDE pulse to get the code onto the RD buss and stuff it into the register on the DDI. At about the same time, the control logic is coerced into state C1 and a one-microsecond pulse on the ULI's SATNO input alerts the computer that the data are ready.

An interrupt service routine then executes instructions--see the software example--so that the ULI outputs shown in Figure 4-22 are generated. The control logic threads its way through states not reached in any other operation, while DINS changes to one and two for the first time in any example. The latter event gives the ULI data inputs access (through the multiplexer) to YC and the eight least significant bits of XC which are



EXAMPLE 6 - CURSOR DATA ENTRY (Same as Cursor Data Entry Example in Table 2 of AJJ-21 in the Appendix)  
NOTE: Time scale varies along abscissa.

Figure 4-22. Cursor Data Entry Timing

not allowed to change at this time since SDG is still true. When all data have been obtained, the computer terminates the operation by producing a CMG pulse, together with a 010X111X command byte, to force the control logic back to state I while resetting SDG by means of the RSDG signal. The SD indicator persists in its on state for an additional half-second so that it can be seen even when the wait for a MATCH is of short duration. A machine-language program for the Interdata 7/32 which facilitates testing the Cursor Data Entry operation of the DDI has been included as Appendix D.

#### 4.7.8 Hardware Test Switch

Located in C26 of the DDI card, this eight-circuit switch permits certain tests to be performed on the DDI without the ULI. The switch and its capabilities are illustrated in Figure 4-23.

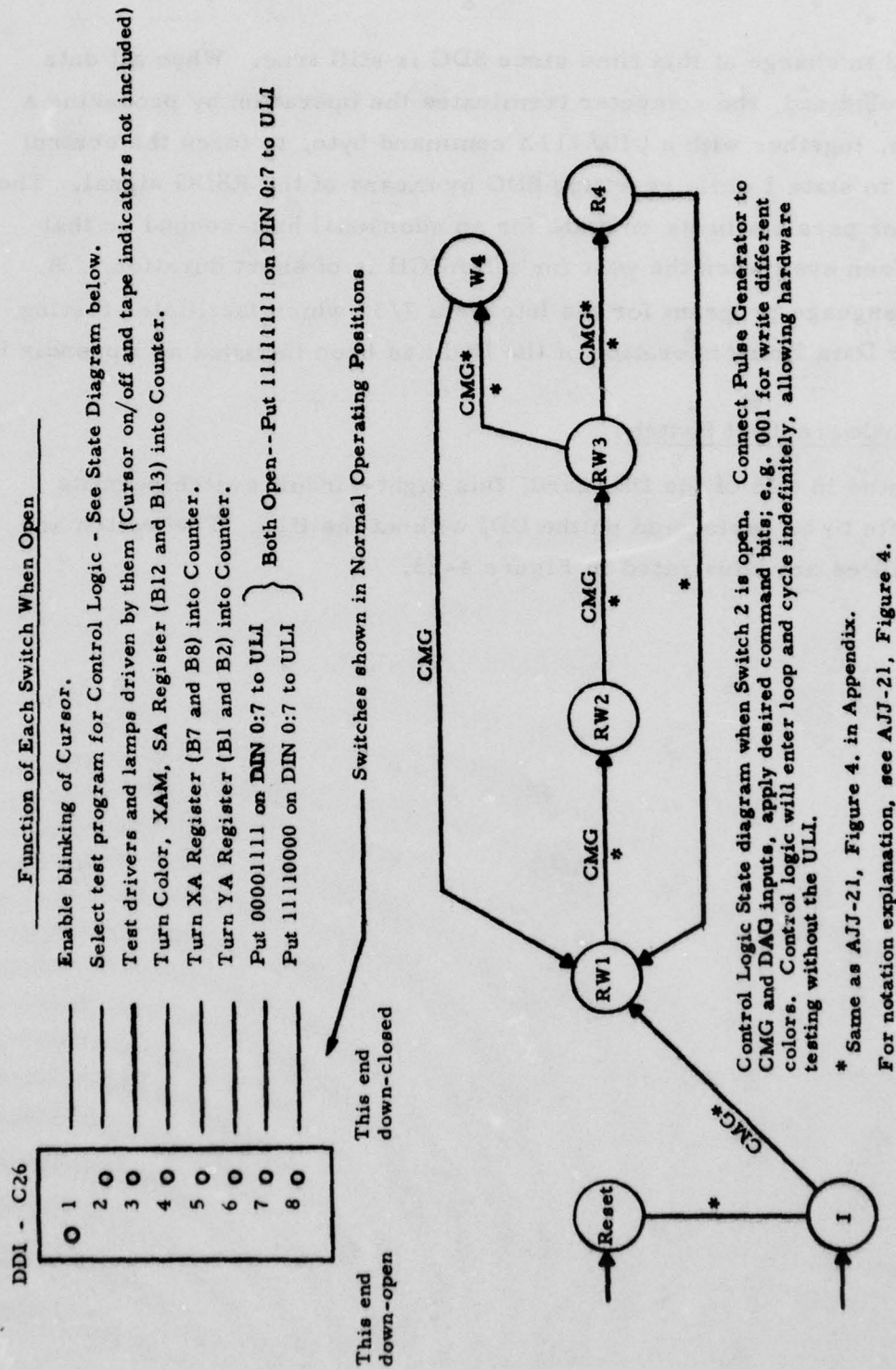


Figure 4-23. Hardware Test Switch

## SECTION 5. DETAILED CIRCUIT DESCRIPTION- REMOTE RECEIVER UNIT

A block diagram of the RRM (Remote Refresh Memory) is included in Figure 2-1. This section describes the DRU and MIU circuitry in detail.

### 5.1 Display Receiver Unit

#### 5.1.1 Timing and Control Logic

Figure 5-1 presents the DRU block diagram, where it can be seen that all timing waveforms are obtained by frequency division of the 11.958041 MHz crystal-controlled clock in the timing and control circuitry below the dashed line. Discussion of the outputs of the clock generator, except for R, is postponed until the section on the MIU where these signals are used.

The square-wave R, with a period of 1.6725 microseconds, is illustrated along the X-axis of Figure 4-8, which shows the display format along with waveforms. Along the X-axis, the display is organized into ten-point blocks designated DXB0 through DXB31; each period of R corresponds to one block. Since each point requires four-bits for color/intensity coding, 40 bits are needed to specify each block. A memory with 40-bit words at consecutive addresses describe a line, and 8192 words contain the entire image.

In order to refresh the display, the memory is sequentially read while the CRT beam scans out a raster; this read cycle is always done while R is high, when the memory address multiplexer (see Figure 5-1 ) routes DXB and DY from the synchronous scan counters to the 13-bit memory address buss. During the remaining half cycle of R, if a store command is received, data are written into the memory at an address (RXB, RYB), where RXB is a 5-bit block select code developed directly in a counter, thereby eliminating the code conversion ROM needed in the MAG of the Master SCRM. As is described in the MIU section, RXP determines which one of the ten points within the block is to be changed.

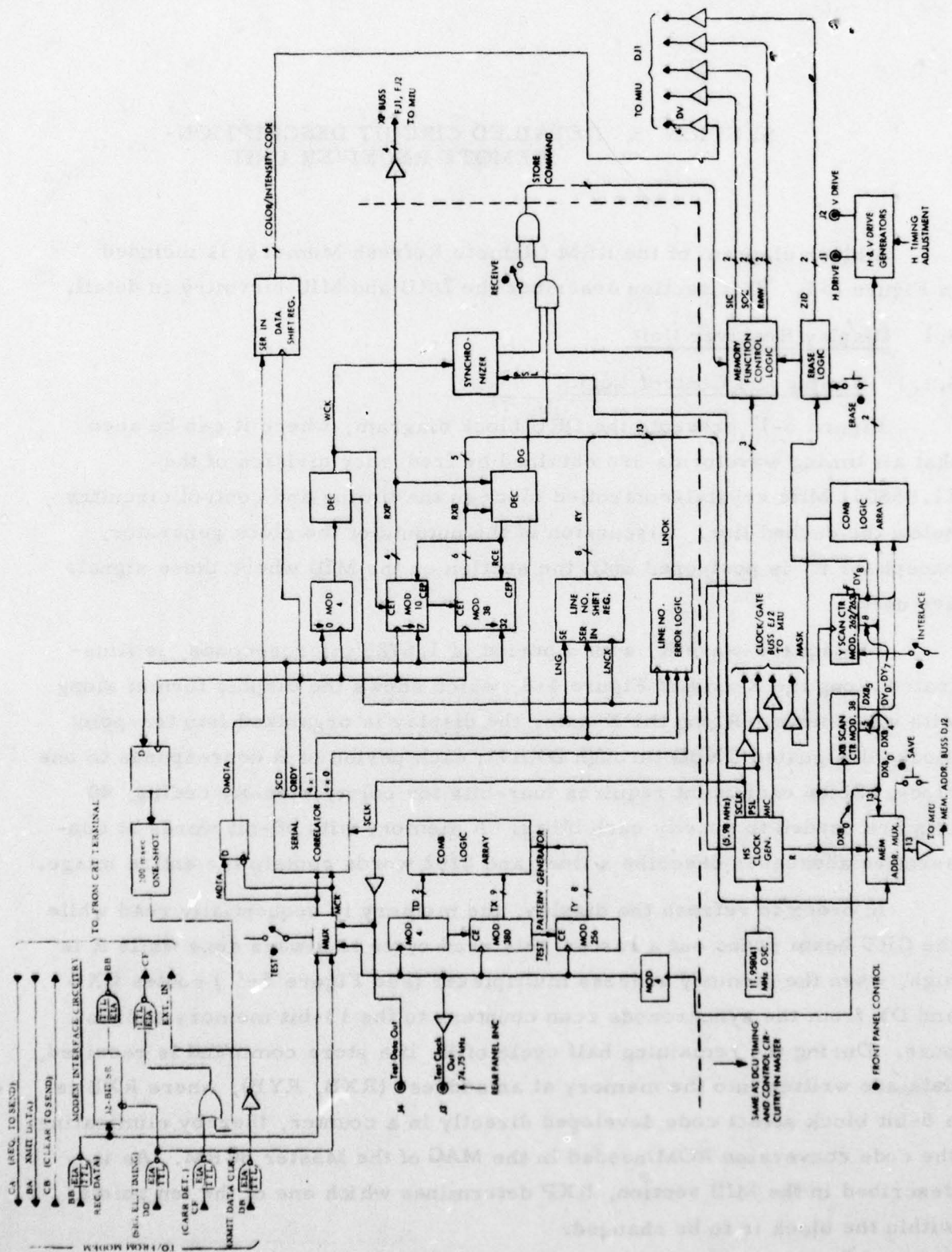


Figure 5-1. DRU (Display Receiver Unit) Block Diagram

The logic array generates waveforms, shown in Figure 4-8, which are functions of the scan counter outputs, DXB or DY. Waveforms which need to be functions of both DXB and DY are derived from them; for example:  $PA = PA(X) \cdot PA(Y)$ . The logic array is implemented with two 32 x 8 PROMs (Programmable Read Only Memories) and a collection of decoders and gates. A truth table for these PROMs, C16 and D20, is tabulated in Appendix B, while the addressing and output waveforms are illustrated in Figure 4-8. The same mask as is used in the Master SCRM is also used in this unit. The effect of this mask can be seen when the test pattern is entered into the display memory of the RRM. Since this mask does not include DA' (see Figure 4-8), when a THI is transmitted from the Master, DA' in the RRM will contain old RHI or PPI data unless the Master's display had been erased before the THI display was started.

Interlaced scanning, possibly useful to fill interline gaps for photographic purposes, or to interface with a system requiring a standard 525-line scan, can be enabled by the front-panel INTERLACE switch. The waveforms which result are shown in Figure 4-8. Timing of the H-drive pulse is adjustable over a range of  $\pm 3$  microseconds by means of a potentiometer; this adjustment can be used to center the image in the raster of the display.

The memory function control logic generates SIC, SOC and RMW signals (to be discussed in the MIU section) which initiate various types of cycles in the memory. The erase logic generates properly timed ZID signals which cause all zeroes (black) to be written into the memory at all addresses.

### 5.1.2 MODEM Interface Circuitry

The collection of level translators and logic at the upper right of Figure 5-1 serves to interface between the MODEM, the CRT terminal, and the DRU. During reception of data from the MASTER SCRM, the 200 msec retriggeable one-shot is kept on by the sequence of detected sync. codes, thereby disabling transmission to the CRT terminal.

### 5.1.3 Test Pattern Generator

The test pattern generator obtains its 74.75 kHz clock by dividing  $DXB_0$  of the XB scan counter by four. The TD, TX and TY counters simulate the corresponding counters in the Master SCRM. They drive a combinatorial logic array which develops the test pattern, including sync. code and line number. This logic array uses a 32 x 8 PROM having the same pattern (Appendix B, DRU D30) as that used in the Master SCRM and in the serial correlator (to be described) of the DRU.

### 5.1.4 Receiver Counters and Registers

The serial correlator will be described in another section. But for the purposes of this section, its outputs are diagrammed in Figure 5-2 which will help to explain operation of the remaining portions of Figure 5-1. It might also be helpful to refer to Figure 4-16 of the Master SCRM section, which describes the serial data format. The ORDY output of the correlator goes high when its other outputs are valid; it is used as a bit clock in the DRU. The serial input data delayed one clock period, DMDTA, is shifted into a 4-bit serial/parallel converter, the output of which is the color-intensity code to be stored in the memory. The RXP and RXB counters, properly initialized by SCD when the correlator finds a sync. code, develop X-addresses at which to store the color/intensity code. The command to store is issued at the proper time as determined by the synchronizer (see bottom of Figure 5-2) but only during the data gate DG. After detection of the sync. code, the line number gate LNG goes high and the line number code is shifted into its register to serve as the Y-address RY. Should there be an error in any bit of the line no. code, LNOK goes low and no store commands are issued until the next successful line.

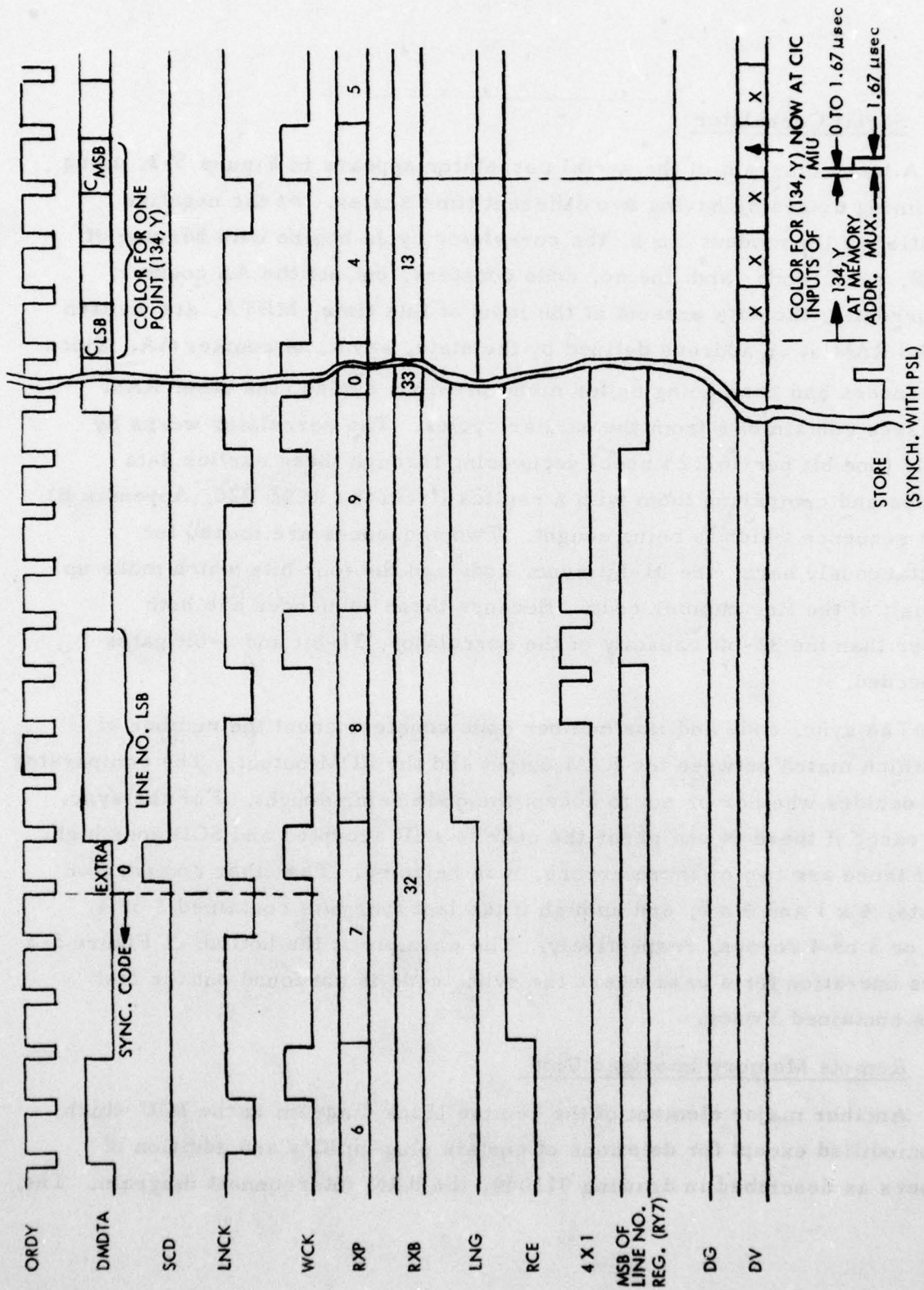


Figure 5-2. DRU Timing Diagram

### 5.1.5 Serial Correlator

A block diagram of the serial correlator appears in Figure 5-3, along with timing diagrams having two different time scales. At the negative transition of the modem clock, the correlator cycle begins with zeroing of the AB, sync. code, and line no. code counters, but not the AA counter. Concurrently, the data present at the input at this time, MDTA, are written into the RAM at an address defined by the state, say K, of counter AA. Since this process had been going on for many previous cycles, the other RAM addresses contain bits from the earlier cycles. The correlator works by rapidly (one bit per 167.25 nsec) sequencing through these earlier data samples and comparing them with a replica (from the ROM B20, Appendix B) of the sequence which is being sought. Two sequences are looked for simultaneously here: the 31-bit sync. code and the four bits which make up one digit of the line number code. Because these sequences are both shorter than the 32-bit capacity of the correlator, 31-bit and 4-bit gates are needed.

The sync. code and line number code counters count the number of bits which match between the RAM output and the ROM output. The comparator logic decides whether or not to accept the code being sought. For the sync. code case, if there is one error the code is still accepted and SCD goes high. But if there are two or more errors, it is rejected. The other comparator outputs, 4 x 1 and 4 x 0, end up high if the last four bits contained 3 or 4 ones or 3 or 4 zeroes, respectively. The example at the bottom of Figure 5-3 shows operation for a case where the sync. code is not found but the last 4 bits contained 3 ones.

### 5.2 Remote Memory Interface Unit

Another major element of the remote block diagram is the MIU which is unmodified except for deletions of certain plug-in IC's and addition of jumpers as described in drawing 911049, the RRM interconnect diagram. The

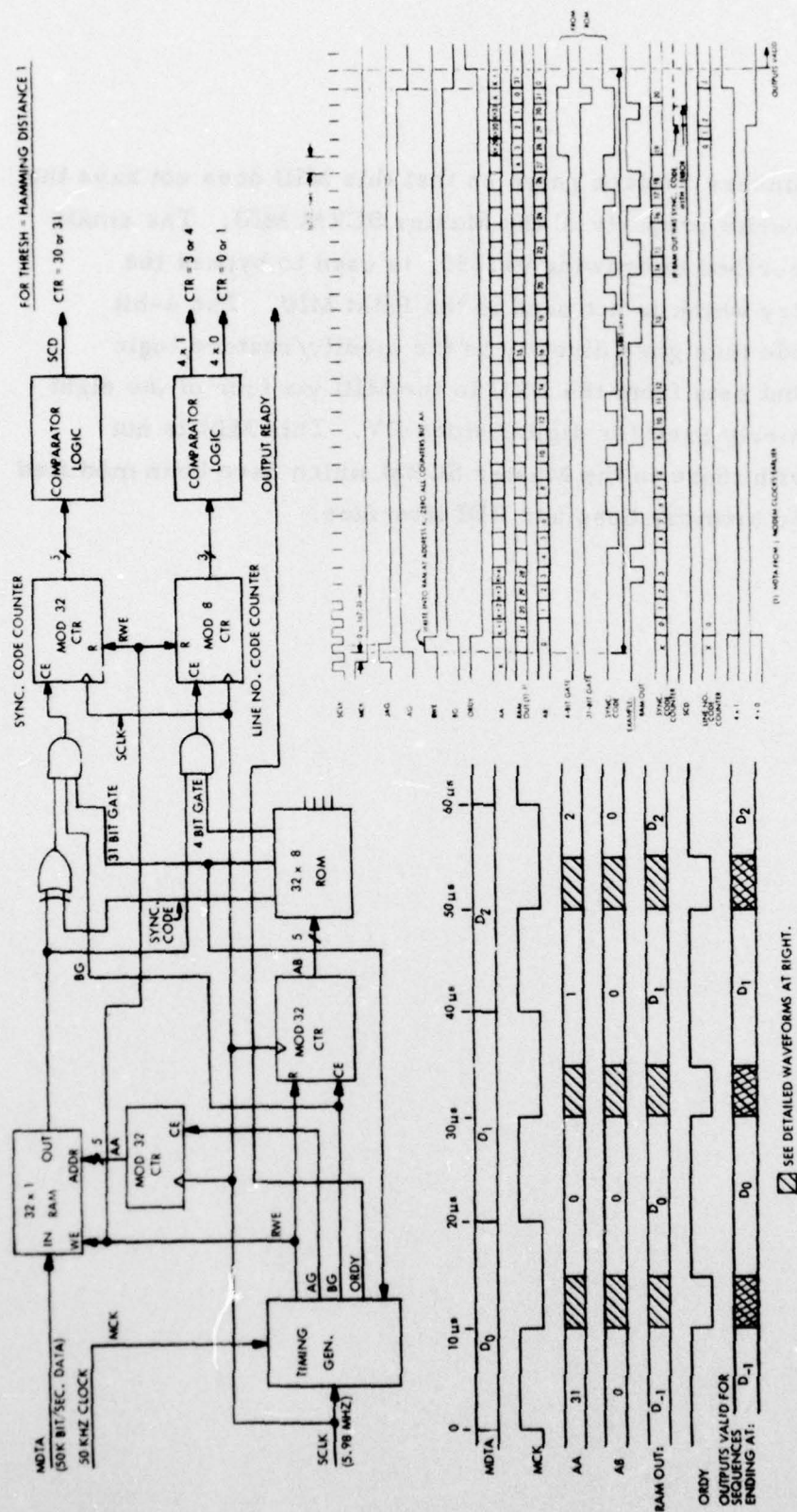


Figure 5-3. Serial Correlator and Waveforms

ten single-wire jumpers replace gates so that this MIU does not have the color 15 non-overwrite property of the Master SCRM MIU. The small jumper cable, described in drawing 911155, is used to bypass the contouring circuitry which is not used in the RRM MIU. The 4-bit color/intensity code thus goes directly to the modify/restore logic (see Figure 5-4) but gets from the DRU to the MIU via four of the eight twisted pairs formerly used for digital video DV. This MIU is not interchangeable with those in the Master SCRM which have been modified for the multiplexed memory buss and DDI interface.

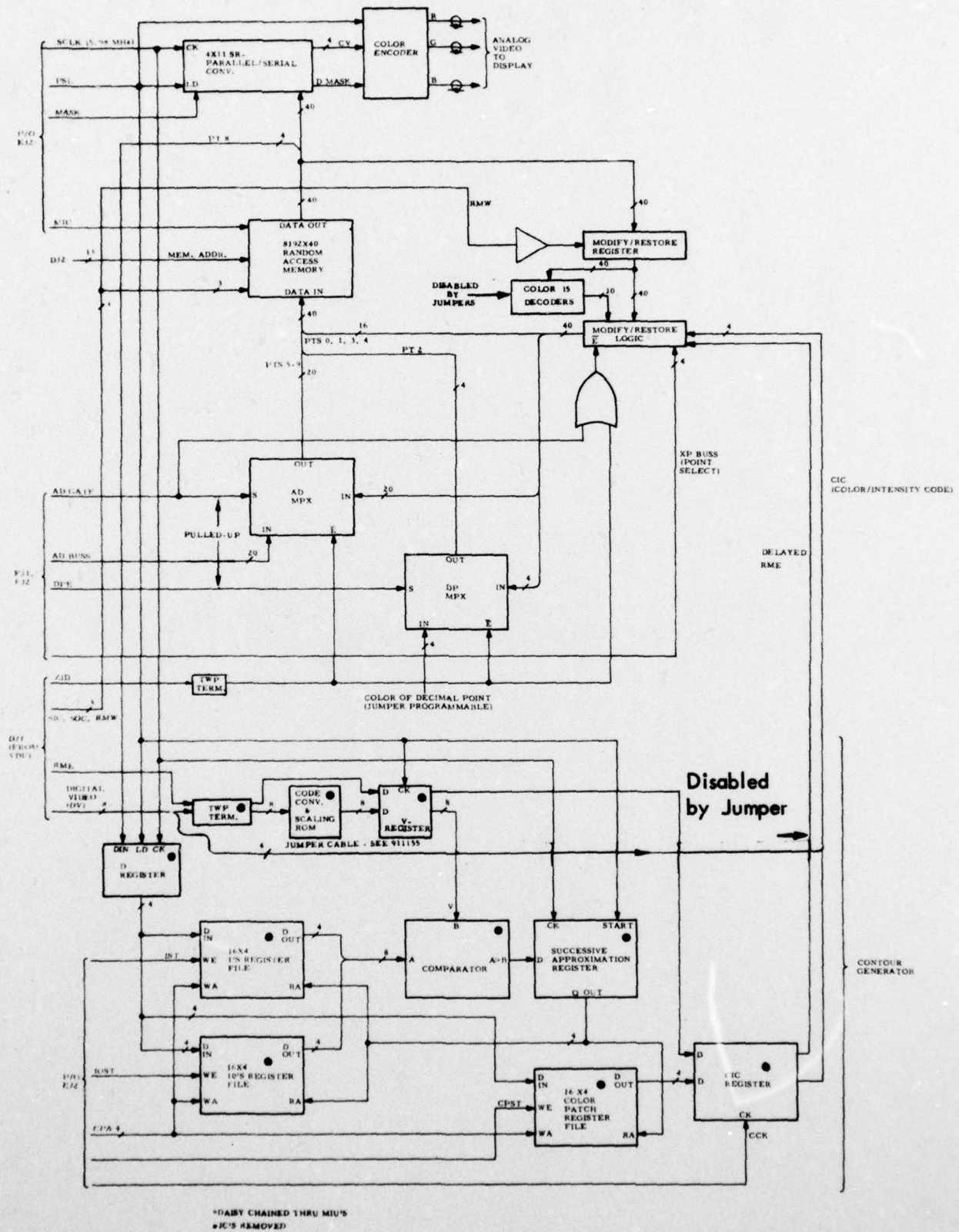
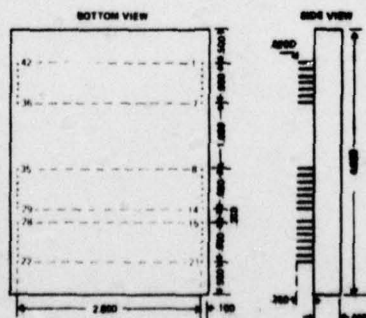
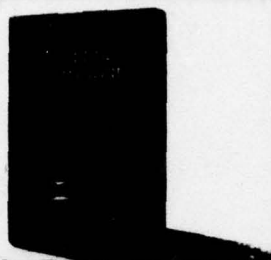


Figure 5-4. Memory Interface Block Diagram (Remote)

## APPENDIX A

### PRODUCT INFORMATION ON SUB-SYSTEM MODULES



FUNCTION		FUNCTION	
PIN	180	PIN	180
8-Bit 2	20	80	2
8-Bit 4	18	40	4
8-Bit 5	16	20	40
8-Bit 6	15	10	17
8-Bit 7	12	6	26
8-Bit 8	11	5	27
8-Bit 9	7	2	31
8-Bit 10	6	1	35
8-Bit 11	4	8	34
8-Bit 12	3	4	36
8-Bit 13	24	2	9
8-Bit 14	25	1	8
8-Bit 15	26	0	27
Load*	17	0	31
+5 VDC	14	02	37
Common	10	01	38

Notes: \* = 6 entry, \*\* = 4 entry

## INTERFACE ENGINEERING



INCORPORATED  
STOUGHTON, MASSACHUSETTS



## DIGITAL TRANSLATOR

BINARY ANGLE  
TO  
BINARY SINE  
MODEL DD108

### DESCRIPTION

The DD108 angle translators are purely digital devices which convert a binary input angle to the corresponding sine of the angle over an input angular range of  $90^\circ$  or, when operated with external quadrant and complementing logic, provide 4 quadrant operation with both sine and cosine digital outputs. (Refer to Bulletin 271007).

The translators employ parallel ripple-thru memories and interpolation logic providing a translation speed limited only by propagation delays. The translation speed, faster than equivalent computer operations, permits the translator to be time shared between using hardware providing the inherent precision of digital processing without tying up a general purpose computer on costly repetitive angle translation routines. Alternatively, the translators avoid the costs and accuracy degradation inherent in analog trig function generators. Both models provide a translation precision of 16 bits. The input resolution of the DD108-A is  $.088^\circ$  and the input resolution of the DD108-B is  $.011^\circ$ .

Input and output logic levels are DTL/TTL compatible. The translators are packaged in compact fully encapsulated low profile cubes. Pins are arranged as in-line groups of 7 on .100 centers permitting direct plug-in to wire wrap planes or PC boards.



INTERFACE ENGINEERING INC.  
306 LINDELOF AVENUE BOX 360  
STOUGHTON, MASSACHUSETTS  
Call (617) 344-7303

### FEATURES

- ☐ FAST 0.75 and 1.2  $\mu$ sec.
- ☐ FINE  $.088^\circ$  and  $.011^\circ$  steps
- ☐ PRECISE - 16 bit output
- ☐ ACCURATE -  $.005^\circ$  arctan

### APPLICATIONS

- SYNCHRO CONVERSION
- COORDINATE TRANSLATION
- SIGNAL PROCESSING
- RESOLVER COMPUTATION
- PATTERN GENERATORS

### SPECIFICATIONS

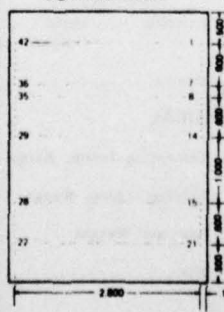
#### ELECTRICAL

DD 108-A INPUT	10 bit binary angle, MSB = $45^\circ$ LSB = $.088^\circ$
DD 108-B INPUT	13 bit binary angle, MSB = $45^\circ$ LSB = $.011^\circ$
DIGITAL OUTPUT	16 bit binary magnitude Sine or Cosine
ANGULAR RANGE	$90^\circ$ (Refer to bulletin 271007 for Sine and Cosine operation over $360^\circ$ range)
TRANSLATION ACCURACY	$\pm .015\%$ of full scale $\pm .005^\circ$ arc (Sin/Cos)
PROPAGATION DELAY	0.75 microseconds DD 108-A 1.20 microseconds DD 108-B
LOGIC	Positive true, DTL/TTL compatible True = + 2.0V to + 5.5V False = 0V to 0.8V
LOADING - Input	8 TTL loads max
Output	2 TTL loads max.
POWER - DD 108-A	+ 5 VDC $\pm 5\%$ @ 600 ma
DD 108-B	+ 5 VDC $\pm 5\%$ @ 800 ma

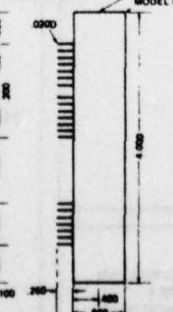
#### PHYSICAL

OPERATING TEMP. RANGE	0 to $70^\circ$ C
STORAGE TEMP. RANGE	$-54$ to $+125^\circ$ C
SIZE AND WEIGHT	DD 108-A.....3"W x 4"L x 0.4"H, 5 ounces DD 108-B.....3"W x 4"L x 0.8"H, 10 ounces
PINS	.020" round, gold plated, .250" L min.

#### BOTTOM VIEW



#### SIDE VIEW



MODULE INPUT OUTPUT CONNECTIONS			
FUNCTION	PIN	FUNCTION	PIN
Bus 1 - MSB 45	16	Bus 12 - Sine	40
Bus 4 -	13	Bus 13 - Cos	41
Bus 5 -	18	Bus 14 - Sine	42
Bus 6 -	5	Bus 15 - Cos	43
Bus 7 -	6	Bus 16 - Sine	44
Bus 8 -	7	Bus 17 - Cos	45
Bus 9 -	2	Bus 18 - Sine	46
Bus 10 -	3	Bus 19 - Cos	47
Bus 11 -	4	Bus 20 - Sine	48
LSB - Sine x 8	9	Bus 21 - Cos	49
Bus 12 -	12	Bus 22 - Sine	50
Bus 13 -	11	Bus 23 - Cos	51
Bus 14 -	14	Bus 24 - Sine	52
Bus 15 -	15	Bus 25 - Cos	53
+5 VDC	10 - 42	Bus 26 - Sine	54
Ground	10 - 26	Bus 27 - Cos	55

\*Note: DD 108-B Model Only

## INTERFACE ENGINEERING



INCORPORATED  
STOUGHTON, MASSACHUSETTS



## DIGITAL TRANSLATOR BINARY ANGLE TO SIN/COS CONTROLLER MODEL DD 109

### DESCRIPTION

The DD109 Binary Angle to Sine and Cosine Controllers adapt the Model DD108 Binary Angle to Binary Sine translators to full four quadrant sine and cosine operation.

The controllers are purely digital devices which determine the quadrant in which the angle lies, determine the polarity of the sine and cosine outputs from the DD108, and route either the input angle or it's two's complement to the input of the DD108. Inhibit logic is provided for forbidden two's complement codes.

A single control line selects the sine or cosine output function. When the line is Low the combined output 17 bit code represents the sign and magnitude of the Sine of the input angle. When the line is High the output 17 bits represent sign and magnitude of the Cosine of the input angle.

The DD109 will accept up to 15 bits in binary angle and can be used with either the DD108A (.088° LSB) or DD108B (.011° LSB).



INTERFACE ENGINEERING INC.  
386 LINDELOF AVENUE  
STOUGHTON, MASSACHUSETTS  
CMI (617) 344-7383

### FEATURES

(With DD108 Angle to Sine Translator)

- ☐ FOUR QUADRANT OPERATION
- ☐ BOTH SINE AND COSINE OUTPUTS
- ☐ 12 OR 15 BIT ANGLE IN
- ☐ 17 BIT SIGN AND MAGNITUDE OUT
- ☐ ACCURACY  $\pm 0.005^\circ$  ARCTAN

### APPLICATIONS

- SYNCHRO CONVERSION
- SIGNAL PROCESSING
- COORDINATE TRANSLATION
- COORDINATE TRANSLATION
- PATTERN GENERATORS

### SPECIFICATIONS

#### ELECTRICAL

Digital Input ..... 15 bit angle (MSB =  $180^\circ$ )

#### Function Select

Sine ..... select line low (0)  
Cosine ..... select line high (1)

#### Digital Outputs

	Quadrant			
	I	II	III	IV
Polarity (Direct Output).....	1	0	1	1
Sine Polarity .....	0	0	1	1
Cosine Polarity .....	0	1	1	0

#### Angle to DD108 (MSB = $45^\circ$ )

Sine Select .....  $90^\circ - \ominus$      $90^\circ - \ominus$      $90^\circ - \ominus$      $90^\circ - \ominus$   
Cosine Select .....  $90^\circ - \ominus$      $\ominus$      $90^\circ - \ominus$      $\ominus$

#### Translation Accuracy (With DD108)

Magnitude .....  $\pm 0.15\%$   
Arc Sin/Cos Ratio .....  $\pm 0.005^\circ$

Propagation Delay..... 0.95  $\mu$ sec with DD108A  
1.50  $\mu$ sec with DD108B

Logic..... Positive true, DTL/TTL compatible  
True = +2.0V to +5.5V  
False = 0 to 0.8V

Loading ..... Input ..... 3 TTL loads max.  
Output..... 10 TTL loads max.

Power..... +5 VDC  $\pm 5\%$  @450 ma

#### PHYSICAL

Operating Temp. Range ..... 0 to  $70^\circ\text{C}$

Storage Temp. Range .....  $-62$  to  $+125^\circ\text{C}$

Size and Weight ..... 2"W x 4"L x 0.4"H, 4 oz.

Pins ..... .020" round, gold plated  
250" L min.

AD-A050 174

RAYTHEON CO WAYLAND MASS ADVANCED DEVELOPMENT LAB  
SCAN CONVERTER AND REFRESH MEMORY WITH REMOTE TERMINAL AND DISP--ETC(U)  
AUG 76 A J JAGODNIK, L R NOVICK

F/G 5/8

F19628-76-C-0101

UNCLASSIFIED

ER76-4227

AFGL-TR-76-0301

NL

2 OF 2

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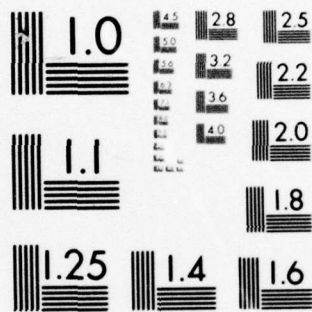
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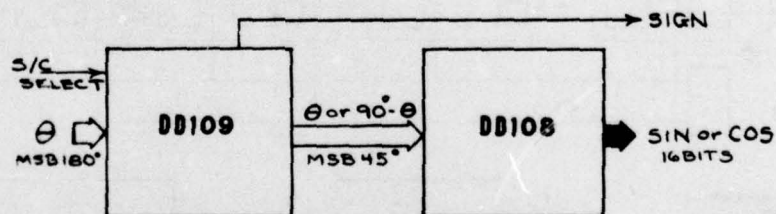
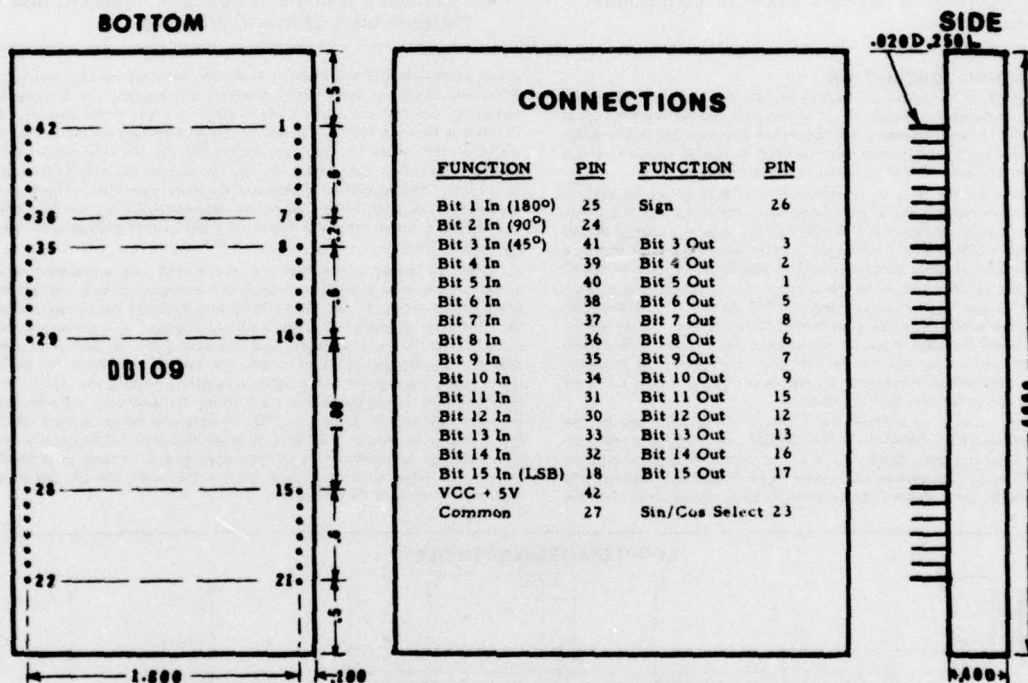


MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS-1963-A

**INTERFACE  
ENGINEERING**



angle measurement and control



**APPLICATION  
ASSISTANCE (617) 344-7383**

**INTERFACE ENGINEERING INC.**

388 LINDELOF AVENUE  
STOUGHTON, MASS. 02072

# Am2502/2503/2504

Eight-Bit/Twelve-Bit Successive Approximation Registers  
Advanced Micro Devices  
Complex Digital Integrated Circuits



## Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel counter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

## FUNCTIONAL DESCRIPTION

The Am2502, Am2503 and Am2504 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

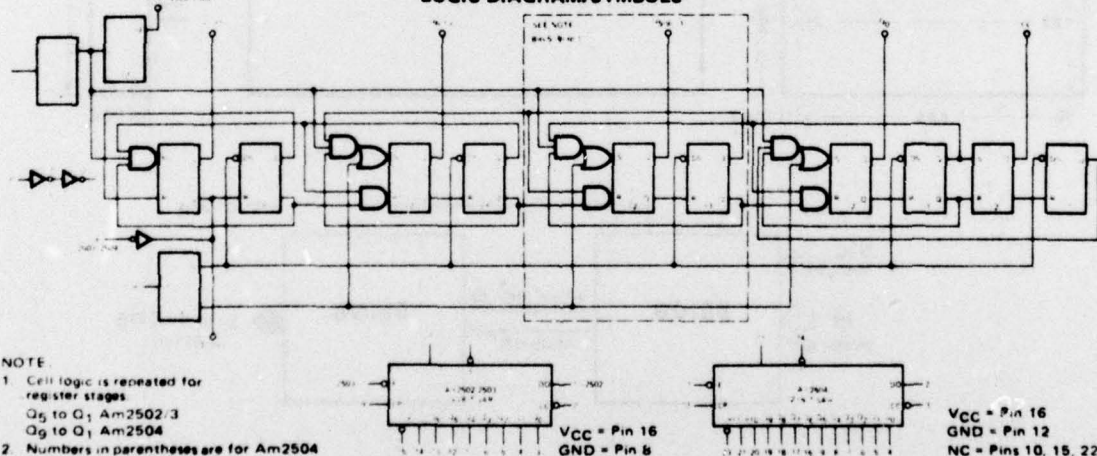
The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am2502 and Am2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the  $\bar{S}$  (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state  $Q_7(11)$  LOW, (Note 2) and all the remaining register outputs HIGH. The  $\bar{C}\bar{C}$  (Conversion Complete) signal is also set HIGH at this time. The  $\bar{S}$  signal should not be brought back HIGH until after the

clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the  $\bar{S}$  signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the  $Q_7(11)$  register bit and the  $Q_6(10)$  register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the  $Q_6(10)$  register bit and  $Q_5(9)$  is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into  $Q_0$ , the  $\bar{C}\bar{C}$  signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input,  $\bar{E}$ , on the Am2503 and Am2504 allows devices to be connected together to form a longer register by connecting the clock, D, and  $\bar{S}$  inputs together and connecting the  $\bar{C}\bar{C}$  output of one device to the  $\bar{E}$  input of the next less significant device. When the Start signal resets the register, the  $\bar{E}$  signal goes HIGH, forcing the  $Q_7(11)$  bit HIGH and inhibiting the device from accepting data until the previous device is full and its  $\bar{C}\bar{C}$  goes LOW. If only one device is used the  $\bar{E}$  input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the  $\bar{C}\bar{C}$  signal to indicate the end of conversion.

## LOGIC DIAGRAM/SYMBOLS



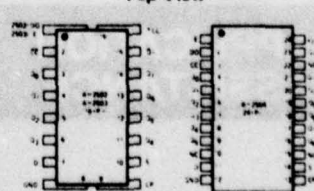
## ORDERING INFORMATION

Package Type	Temperature Range	Am2502 Order Number	Am2503 Order Number	Am2504 Order Number
Molded DIP	0°C to +75°C	AM2502PC	AM2503PC	AM2504PC
Hermetic DIP	0°C to +75°C	AM2502DC	AM2503DC	AM2504DC
Hermetic DIP	-55°C to +125°C	AM2502DM	AM2503DM	AM2504DM
Hermetic Flat Pak	-55°C to +125°C	AM2502FM	AM2503FM	AM2504FM
Dice	Note	AM2502XX	AM2503XX	AM2504XX

NOTE: The dice supplied will contain units which meet both 0°C to +75°C and -55°C to +125°C temperature ranges.

## CONNECTION DIAGRAMS

Top View



NOTE: PIN 1 is marked for orientation.

**MAXIMUM RATINGS** (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	-0.5 V to +V <sub>CC</sub> max
DC Input Voltage	-0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	-30 mA to +5.0 mA

**ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (Unless Otherwise Noted)

Am2502XC    Am2503XC    Am2504XC    T<sub>A</sub> = 0°C to +75°C    V<sub>CC</sub> = 5.0V ±5%  
 Am2502XM    Am2503XM    Am2504XM    T<sub>A</sub> = -55°C to +125°C    V<sub>CC</sub> = 5.0V ±10%

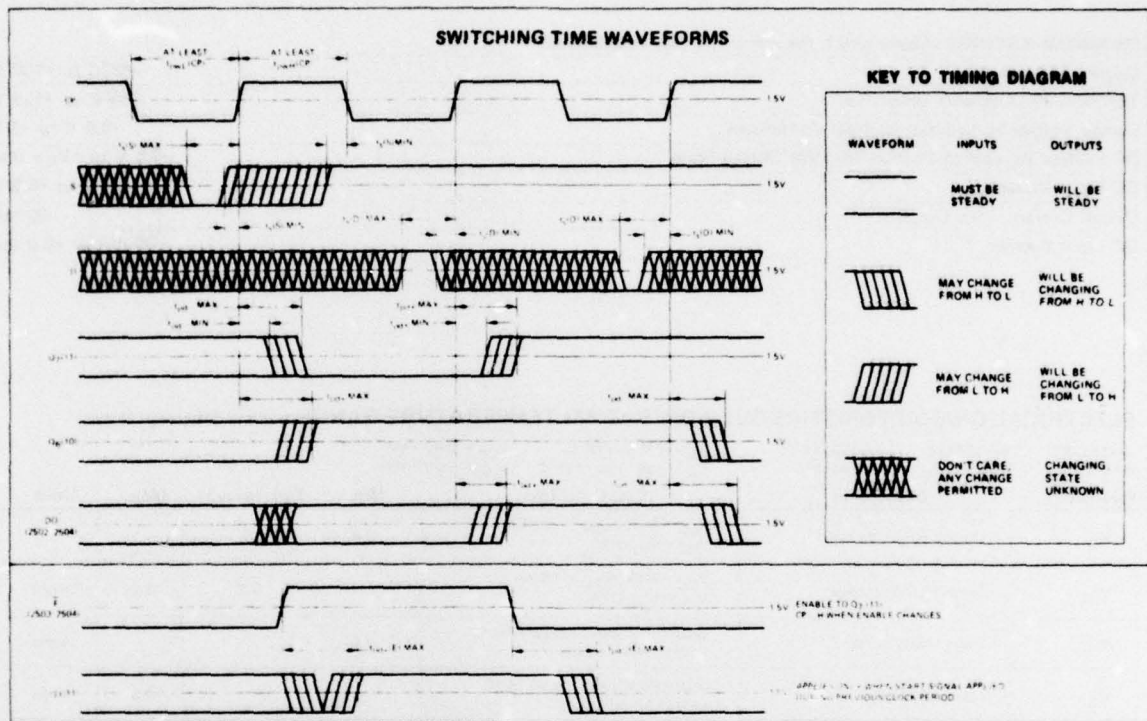
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = MIN., I <sub>OH</sub> = -0.48mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4	3.6		Volts
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = MIN., I <sub>OL</sub> = 9.6mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		0.2	0.4	Volts
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I <sub>IL</sub> (Note 2)	Unit Load Input LOW Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 0.4V		-1.0	-1.6	mA
I <sub>IH</sub> (Note 2)	Unit Load Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 2.4V		6.0	40	μA
	Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 5.5V			1.0	mA
I <sub>SC</sub>	Output Short Circuit Current	V <sub>CC</sub> = MAX., V <sub>OUT</sub> = 0.0V	-10	-25	-45	mA
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = MAX.	Am2502		65	85
					65	95
			Am2503		60	80
					60	90
			Am2504		90	110
					90	124

Note 1. Typical Limits are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading.

2. Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

**Switching Characteristics** T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V, C<sub>L</sub> = 15 pF

Parameters	Description	Min.	Typ.	Max.	Units
t <sub>pd+</sub>	Turn Off Delay CP to Output HIGH	10	26	38	ns
t <sub>pd-</sub>	Turn On Delay CP to Output LOW	10	18	28	ns
t <sub>s(D)</sub>	Set-up Time Data Input	-10	4	8	ns
t <sub>s(S)</sub>	Set-up Time Start Input	0	9	16	ns
t <sub>pd+(E)</sub>	Turn Off Delay E to Q <sub>7</sub> (11) HIGH	(Am2503/4) C <sub>p</sub> = H, S = L	13	19	ns
t <sub>pd-(E)</sub>	Turn On Delay E to Q <sub>7</sub> (11) LOW		16	24	ns
t <sub>pwl(CP)</sub>	Minimum LOW Clock Pulse Width		28	46	ns
t <sub>pwl(ICP)</sub>	Minimum HIGH Clock Pulse Width		12	20	ns
f <sub>max</sub>	Maximum Clock Frequency	15	25		MHz



## DEFINITION OF TERMS

### SUBSCRIPT TERMS:

**H** HIGH, applying to a HIGH logic level or when used with  $V_{CC}$  to indicate high  $V_{CC}$  value.

**I** Input

**L** LOW, applying to LOW logic level or when used with  $V_{CC}$  to indicate low  $V_{CC}$  value.

**O** Output

### FUNCTIONAL TERMS:

**Fan-Out** The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

**Input Unit Load** One T<sup>2</sup>L gate input load. In the HIGH state it is equal to  $I_{IH}$  and in the LOW state it is equal to  $I_{IL}$ .

**CP** The clock input of the register.

**CC** The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

**D** The serial data input of the register.

**E** The register enable. This input is used to expand the length of the register and when HIGH forces the Q<sub>7(11)</sub> register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

**Q<sub>7(11)</sub>** The true output of the MSB of the register.

**$\bar{Q}_7(11)$**  The complement output of the MSB of the register.

**Q<sub>i</sub> (i = 7(11) to 0)** The outputs of the register.

**S** The start input. If the start input is held LOW for at least a clock period the register will be reset to Q<sub>7(11)</sub> LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the S input.

**DO** The serial data output. (The D input delayed one bit).

### OPERATIONAL TERMS:

**I<sub>IL</sub>** Forward input load current.

**I<sub>OH</sub>** Output HIGH current, forced out of output  $V_{OH}$  test.

**I<sub>OL</sub>** Output LOW current, forced into the output in  $V_{OL}$  test.

**I<sub>IH</sub>** Reverse input load current.

**Negative Current** Current flowing out of the device.

**Positive Current** Current flowing into the device.

**V<sub>IH</sub>** Minimum logic HIGH input voltage.

**V<sub>IL</sub>** Maximum logic LOW input voltage.

**V<sub>OH</sub>** Minimum logic HIGH output voltage with output HIGH current  $I_{OH}$  flowing out of output.

**V<sub>OL</sub>** Maximum logic LOW output voltage with output LOW current  $I_{OL}$  flowing into output.

**SWITCHING TERMS:** (Measured at the 1.5V logic level).

**t<sub>pd-</sub>** The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

**t<sub>pd+</sub>** The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

**t<sub>pd-(E)</sub>** The propagation delay from the Enable signal HIGH-LOW transition to the Q<sub>7(11)</sub> output signal HIGH-LOW transition.

**t<sub>pd+(E)</sub>** The propagation delay from the Enable signal LOW-HIGH transition to Q<sub>7(11)</sub> output signal LOW-HIGH transition.

**t<sub>s(D)</sub>** Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t<sub>s</sub> max. and t<sub>s</sub> min. before the clock.

**t<sub>s(S)</sub>** Set-up time required for a LOW level to be present at the S input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

**t<sub>pw(CP)</sub>** The minimum clock pulse width (LOW or HIGH) required for proper register operation.

ATJ

Am2502/3 TRUTH TABLE

Time	Inputs			Outputs											
$t_n$	D	$\bar{S}$	$\bar{E}$	D <sub>0</sub>	Q <sub>7</sub>	Q <sub>6</sub>	Q <sub>5</sub>	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	CC		
0	X	L	L	X	X	X	X	X	X	X	X	X	X		
1	D <sub>7</sub>	H	L	X	L	H	H	H	H	H	H	H	H		
2	D <sub>6</sub>	H	L	D <sub>7</sub>	D <sub>7</sub>	L	H	H	H	H	H	H	H		
3	D <sub>5</sub>	H	L	D <sub>6</sub>	D <sub>7</sub>	D <sub>6</sub>	L	H	H	H	H	H	H		
4	D <sub>4</sub>	H	L	D <sub>5</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	L	H	H	H	H	H		
5	D <sub>3</sub>	H	L	D <sub>4</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	L	H	H	H	H		
6	D <sub>2</sub>	H	L	D <sub>3</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	L	H	H	H		
7	D <sub>1</sub>	H	L	D <sub>2</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	L	H	H		
8	D <sub>0</sub>	H	L	D <sub>1</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	L	H		
9	X	H	L	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	L		
10	X	X	L	X	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	L		
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC		

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

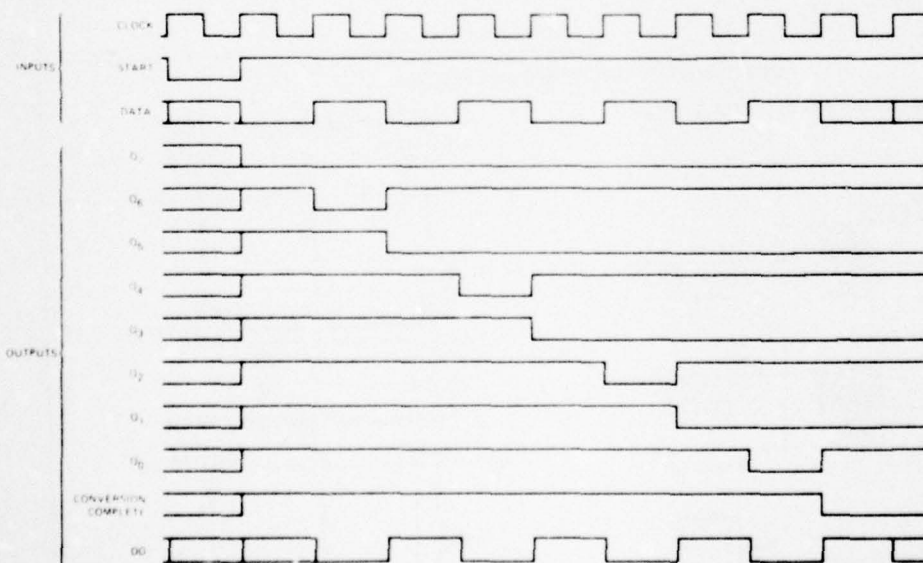
NC = No Change

Note: Truth Table for Am2504 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH, a logic "1" is represented as a high voltage level.
2. For a maximum digital error of  $\pm 1/2$  LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased  $+1/2$  LSB and if the current switches require a high logic level to turn on then the comparator must be biased  $-1/2$  LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can be used to perform 2's complement conversion by offsetting the comparator  $1/2$  full range  $\pm 1/2$  LSB and using the complement of the MSB Q<sub>7</sub> (11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power on. This situation can be overcome by making the START input the OR function of CC and the appropriate register output.

Am2502/3 TIMING CHART



Am2502/3 LOADING RULES (IN UNIT LOADS)					
Input/Output	Pin No.'s	Input Unit Load		Fanout	
		LOW	HIGH	Output HIGH	Output LOW
E (2503)	1	2	2	—	—
DO (2502)	1	—	—	12	6
CC	2	—	—	12	6
Q <sub>0</sub>	3	—	—	12	6
Q <sub>1</sub>	4	—	—	12	6
Q <sub>2</sub>	5	—	—	12	6
Q <sub>3</sub>	6	—	—	12	6
D	7	2	2	—	—
GND	8	—	—	—	—
CP	9	1	1	—	—
S	10	1	2	—	—
Q <sub>4</sub>	11	—	—	12	6
Q <sub>5</sub>	12	—	—	12	6
Q <sub>6</sub>	13	—	—	12	6
Q <sub>7</sub>	14	—	—	12	6
Q <sub>7</sub>	15	—	—	12	6
V <sub>CC</sub>	16	—	—	—	—

Am2504 LOADING RULES (IN UNIT LOADS)					
Input/Output	Pin No.'s	Input Unit Load		Fanout	
		LOW	HIGH	Output HIGH	Output LOW
E	1	2	2	—	—
DO	2	—	—	12	6
CC	3	—	—	12	6
Q <sub>0</sub>	4	—	—	12	6
Q <sub>1</sub>	5	—	—	12	6
Q <sub>2</sub>	6	—	—	12	6
Q <sub>3</sub>	7	—	—	12	6
Q <sub>4</sub>	8	—	—	12	6
Q <sub>5</sub>	9	—	—	12	6
NC	10	—	—	—	—
D	11	2	2	—	—
GND	12	—	—	—	—
CP	13	1	1	—	—
S	14	1	2	—	—
NC	15	—	—	—	—
Q <sub>6</sub>	16	—	—	12	6
Q <sub>7</sub>	17	—	—	12	6
Q <sub>8</sub>	18	—	—	12	6
Q <sub>9</sub>	19	—	—	12	6
Q <sub>10</sub>	20	—	—	12	6
Q <sub>11</sub>	21	—	—	12	6
NC	22	—	—	—	—
Q <sub>11</sub>	23	—	—	12	6
V <sub>CC</sub>	24	—	—	—	—

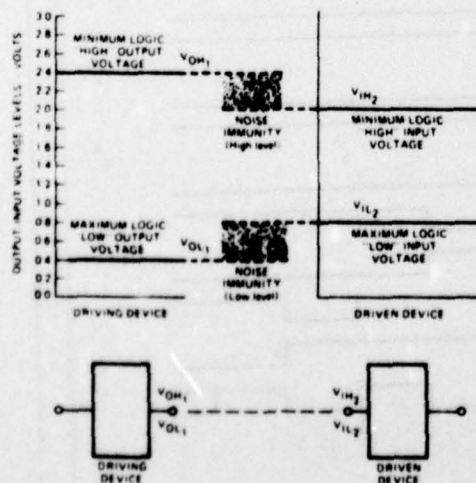
  

MSI INTERFACING RULES			
Interfacing Digital Family		Equivalent Input Unit Load	
		HIGH	LOW
Advanced Micro Devices 9300/2500 Series		1	1
FSC Series 9300		1	1
Advanced Micro Devices 54/7400		1	1
TI Series 54/7400		1	1
Signetics Series 8200		2	2
National Series DM 75/85		1	1
DTL Series 930		12	1

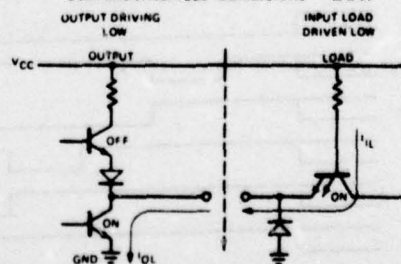
NC = No Connection

### INPUT/OUTPUT INTERFACE CONDITIONS

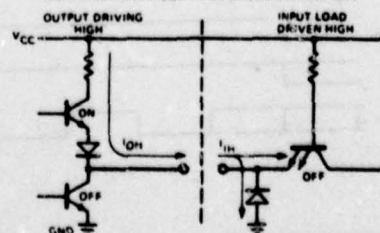
#### Voltage Interface Conditions – LOW & HIGH



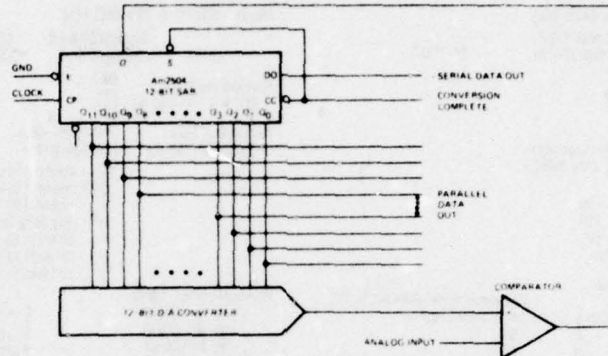
#### Current Interface Conditions – LOW



#### Current Interface Conditions – HIGH



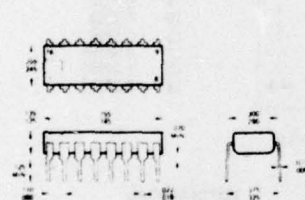
### Am2502/3/4 APPLICATION Continuous Conversion Analog-to-Digital Converter



This shows how the Am2502/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 100,000 conversions per second. A 10-bit continuous conversion can be performed by connecting  $Q_1$  to  $Q_3$  and using  $Q_1$  as the conversion complete signal. The comparator can be the Am111 precision comparator, Am106 high-speed comparator, or Am686 very high speed comparator.

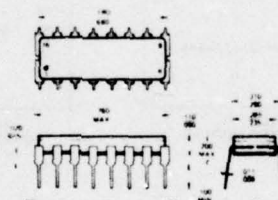
#### Am2502/3

##### 16-Pin Molded DIP

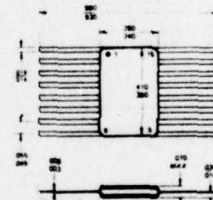


#### PHYSICAL DIMENSIONS

##### 16-Pin Hermetic DIP

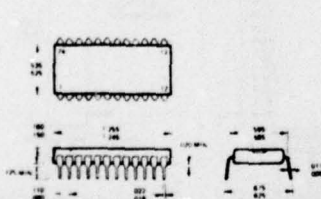


##### 16-Pin Flat Pak

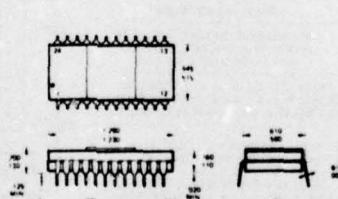


#### Am2504

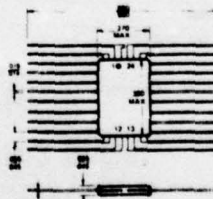
##### 24-Pin Molded DIP



##### 24-Pin Hermetic DIP

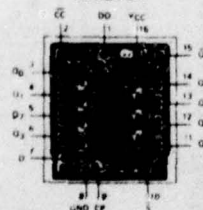


##### 24-Pin Flat Pak



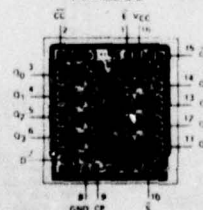
#### Metalization and Pad Layout

##### Am2502



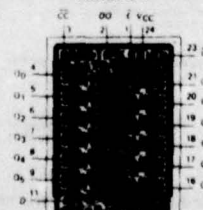
DIE SIZE 0.087 x 0.086

##### Am2503



DIE SIZE 0.087 x 0.086

##### Am2504



DIE SIZE 0.087 x 0.124



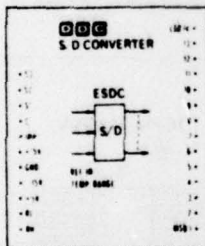
**ADVANCED  
MICRO  
DEVICES INC.**  
901 Thompson Place  
Sunnyvale  
California 94086  
(408) 732-2400  
TWX: 910-339-9280  
TELEX: 34-6306

Advanced Micro Devices can not assume responsibility for use of any circuitry described other than circuitry entirely embodied in an Advanced Micro Devices product.

## PIN DESIGNATIONS AND CONNECTIONS

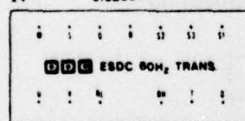
### Models ESDC or ERDC, H or L (400 Hz)

INPUT	CONVERTER CONNECTION	OUTPUT
Synchro input: 11.8V L-L 400 Hz (ESDC-L), or 90V L-L 400 Hz (ESDC-H)	S1 S3 S2	
Reference input: 26V, 400 Hz (ESDC-L), or 115V, 400 Hz (ESDC-H)	RH (high side) RL (low side)	
Power Supplies $\pm 5\%$ : +15V @ 55mA -15V @ 30mA +5V @ 280mA Common	+15V -15V +5V GND	
Logic "0" forces data hold	INH	Converter busy when logic "1"



TOP VIEW OF MODULE

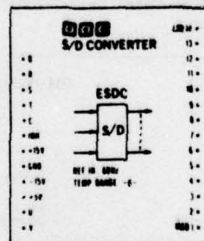
MSB	LSB
1	180° True Logic
2	90
3	45
4	22.5
5	11.25
6	5.625
7	2.813
8	1.406
9	0.7031
10	0.3516
11	0.1758
12	0.08799
13	0.04395
14	0.02197



TOP VIEW OF TRANSFORMER MODULE

### Model ESDC-6 (50-400 Hz)

INPUT	TRANSFORMER CONNECTION	CONVERTER CONNECTION	OUTPUT
Synchro input: 90V L-L 50-400 Hz	S1 S3 S2		
Reference input: 115V 50-400 Hz	RH (high side) RL (low side)		
Power supplies $\pm 5\%$ : +15V @ 75mA -15V @ 50mA +5V @ 400mA Common	R connect to R Q, Q' connect to Q S connect to S W (no connection) T connect to T V connect to V U connect to U	+15V -15V +5V GND	
Logic "0" forces data hold	INH	Converter busy when logic "1"	



TOP VIEW OF CONVERTER MODULE

MSB	LSB
1	180° True Logic
2	90
3	45
4	22.5
5	11.25
6	5.625
7	2.813
8	1.406
9	0.7031
10	0.3516
11	0.1758
12	0.08799
13	0.04395
14	0.02197

## SPECIFICATIONS

### ELECTRICAL

PARAMETER	VALUE
ACCURACY <sup>(1)</sup>	$\pm 4$ minutes $\pm 0.8$ LSB
RESOLUTION	14 Bits
CODING	natural binary 'angle'
DIGITAL OUTPUT	parallel, positive logic, DTL/TTL levels, 14 angle data, 1 inhibit and 1 converter busy line
SYNCHRO INPUT <sup>(2)(3)</sup>	11.8V rms L-L 400 Hz into 10K $\Omega$ min. L-L balanced (ESDC-L) 90V rms L-L 400 Hz into 600K $\Omega$ min. L-L balanced (ESDC-H) 90V rms L-L 50-400 Hz into 4M $\Omega$ min. L-L balanced (ESDC-6)
SYNCHRO INPUT RATES <sup>(4)</sup>	0 to 360°/sec, full accuracy; 180°/sec $\pm 1$ LSB error (ESDC-H or L) 0 to 180°/sec, full accuracy; 6°/sec $\pm 1$ LSB error (ESDC-6)
RESOLVER INPUT <sup>(2)(3)</sup>	11.8V rms L-L 400 Hz into 10K $\Omega$ min. L-L balanced (ERDC-L) 90V rms L-L 400 Hz into 600K $\Omega$ min. L-L balanced (ERDC-H)
RESOLVER INPUT RATES <sup>(4)</sup>	0 to 360°/sec, full accuracy 180°/sec $\pm 1$ LSB error
REFERENCE INPUT <sup>(2)(3)</sup>	26V at 5mA rms 400 Hz (ESDC or ERDC-L) 115V at 0.6mA rms 400 Hz (ESDC or ERDC-H) 115V at 2.5mA rms 50-400 Hz (ESDC-6)
POWER SUPPLY REQUIREMENTS <sup>(5)</sup>	+15V at 75mA, -15V at 50mA, +5V at 400mA

(1) Accuracy applies over operating temperature range,  $\pm 5\%$  variation of power supplies and  $\pm 10\%$  amplitude and frequency variation.  
(2) Other input voltages and frequencies available.  
(3) Transformer isolated.  
(4) Available for use with  $\pm 12V$  supplies.  
(5) 4 R.P.S. available on 400 Hz converters by specifying suffix FT.

### ENVIRONMENTAL

TEMPERATURE RANGES	
OPERATING	-55°C to +85°C (ESDC-H, L, or 6-1) 0°C to +70°C (ESDC-H, L, or 6-3)
STORAGE	-55°C to +125°C

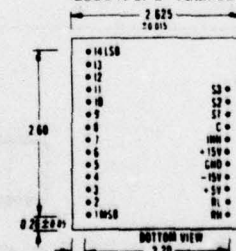
OTHER ENVIRONMENTAL MEETS REQUIREMENTS OF MIL-STD-202C: METHODS 204A, 108B, 107B, 101B and 109.

### ORDERING INFORMATION

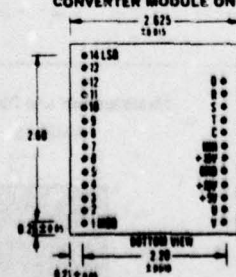
To order, specify model desired followed by the designation of the operating temperature range required (e.g. ESDC-6-1).

### MECHANICAL

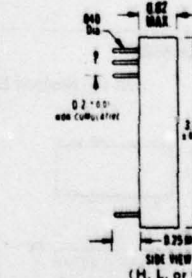
#### ESDC-H or L COMPLETE



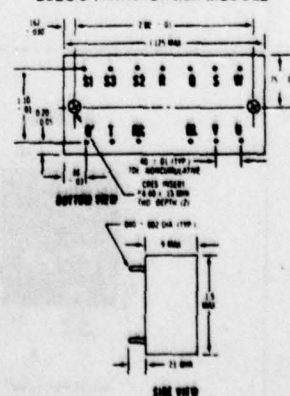
#### ESDC-6 CONVERTER MODULE ONLY



NOTE: In the 400 Hz versions (ESDC-H or L), the resolution transformers are packaged together with the converter in a single module. The 50-60 Hz version (ESDC-6) is supplied in two modules, one for the converter and one for the resolution transformers. Model 9010 mating sock accepts either module but not the 50-60 Hz transformer module.



#### ESDC-6 TRANSFORMER MODULE



### Timing

Figure 6 shows the timing waveforms of the converters. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a CONVERTER BUSY pulse. During the 3  $\mu$ s "busy" pulse, the output data is changing and should not be transferred into the computer output buffer. The converter will ignore an INHIBIT command applied during the "busy" interval until that interval is over. A simple method of interfacing to a computer is to: (a) apply the inhibit, (b) wait 5  $\mu$ s, (c) transfer the data, and (d) release the inhibit.

Although the computer usually will require that the data be synchronized and loaded as described above, it can be read-out asynchronously into a holding register using the trailing-edge of the "C" signal to effect the parallel transfer. This is shown in Fig. 7. In this configuration the data out of the register will change smoothly from  $n$  to  $n + 1$ .

Figure 6: Timing

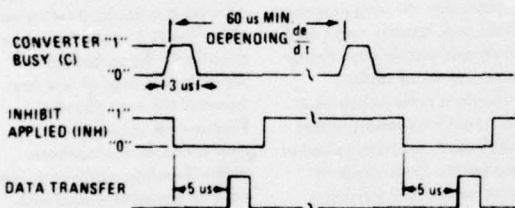


Figure 7: Asynchronous Parallel Transfer

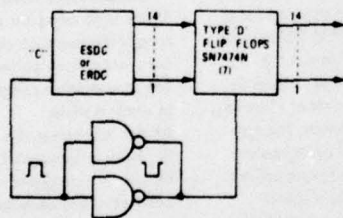
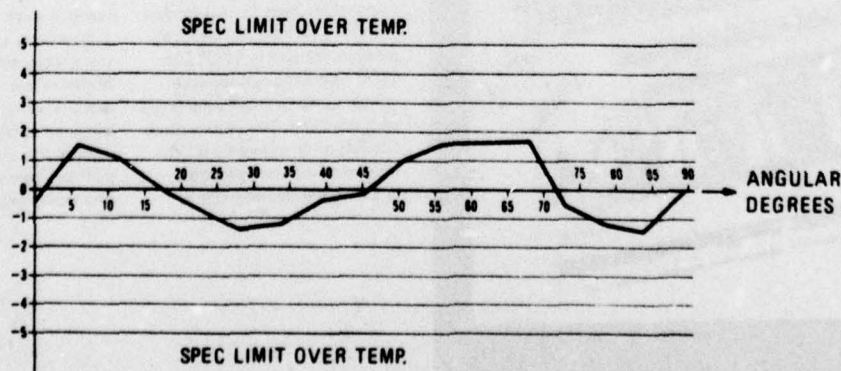


Figure 10: Typical Error, Minutes, Each Quadrant, 25°C for ESDC



### Testing

Because of the high accuracy of these converters, only laboratory-grade synchro or resolver substitution boxes or standards can be used. To avoid costly test equipment, we invite you to use DDC's facilities for "source inspection," at no extra cost.

To test the unit, arrange your test equipment as shown in Figure 8. A lamp-driver or suitable readout is necessary for each of the data outputs. We recommend the circuit shown in Fig. 5C. The Synchro Standard is set to the test angles. The angles corresponding to the lights which are on are added and compared with the standard angle. Maximum observed error shall be less than  $\pm 4$  minutes  $\pm 0.9$  LSB over the temperature range. A table of angles versus bits is given in Fig. 9. A typical room-temperature error curve is shown in Fig. 10. Each quadrant is identical, and error has been shown for the first quadrant. Error limits are also indicated for temperature extremes.

Figure 8: Test Configuration

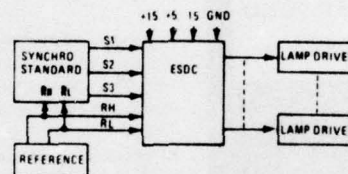


Figure 9: Angles vs. Bits

MSB 1	180
2	90
3	45
4	22.5
5	11.25
6	5.625
7	2.813
8	1.406
9	0.7031
10	0.3516
11	0.1758
12	0.08799
13	0.04395
LSB 14	0.02197

2065

**AMPEX CORE  
MEMORY  
MODULES,  
250 NANOSECOND  
ACCESS AND  
650 NANOSECOND  
CYCLE TIMES**

**Fast and compact**

The Ampex 2065 core memory is faster and more compact than any other 20-bit word length memory available to the OEM. Access time is 250 ns, cycle time 650 ns. It measures only 8 inches high x 10 inches deep x 2 inches wide.

**Unequaled packing density**

You can store more than 160,000 bits in a single 2065 module which occupies only 170 cubic inches in your system. All circuitry is packaged on three removable printed circuit boards—data register, drive, and planar core stack. The compact dimensions of the 2065 provide inherent packaging flexibility which is superior to that of large single board systems. As a result, you have more space available for other important system functions.

**Quality assured reliability**

The 2065 has more built-in reliability than any comparable OEM memory. All critical areas of the memory receive extra attention, and design simplicity is followed throughout. Conservative derating practices, device qualification, and careful component specification further ensure overall reliability. Ruggedized construction used throughout the memory makes it particularly suited to industrial applications. Every stage of the manufacturing process is closely monitored by the Ampex Quality Assurance Department in accordance with MIL-Q-9858A.

**Simple interface,  
easily expandable**

Up to eight 8K x 20 modules can be combined in parallel for a capacity of 65,536 20-bit words. This flexibility permits the addition of memory capacity in increments to meet changing system requirements. Longer words can also be accommodated by combining modules. The use of module select decode and negative-TRUE open collector outputs makes interfacing extremely simple.

**Faster switching,  
broader margins**

The 2065 uses 18-mil temperature stable cores to provide fast switching and broad operating margins across the full 0°C to 55°C operating temperature range. Cooling requirements are also simplified. The planar stack consists of up to twenty 8,192-core mats with an integrated circuit diode decode matrix.

**AMPEX**

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**Maximum output,  
less noise**

Coupled noise is reduced, and a maximum output signal is provided by high density core packaging which permits shorter sense, X and Y lines. Cores are aligned in a double-herringbone pattern with a center-to-center spacing (in the sense/digit winding direction) of less than one-half the core diameter. Precise core alignment is maintained by a proprietary silastic bonding which dissipates core switching heat and minimizes temperature gradients by providing a thermal path to the substrate.

Only two voltages are required +5 and -15.

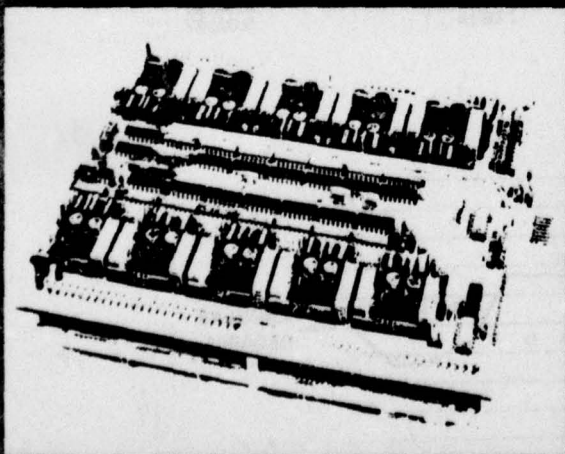
**Temperature compensated**

There is no need for power supply temperature compensation, since drive current sources are temperature compensated in each module.

All the interconnections within the module between circuit boards are provided. No additional low level back panel wiring is required.

**Modular interchangeability**

Complete module-to-module uniformity is provided by optimization of memory timing, drive currents, and threshold levels in each module. Your field support and spares requirements are greatly simplified by the ability to interchange any module within a system or between different systems. Each module is a complete memory with self contained data register and timing and control functions.



2065

# 2065 specifications

Access time	250 nanoseconds
Cycle time	650 nanoseconds
Capacity	2,048, 4,096, 8,192 words of 10, 16, 18 or 20 bits in a single module. Expandable in modules to a capacity of 65,536 words. Longer words can also be accommodated by combining modules.
Operational modes	Read-Restore Clear-Write Read-Modify-Write
Interface characteristics	TTL negative TRUE logic is used.
Standard input signal lines	Address input Data input Start input cycle (SIC) Start output cycle (SOC) Read-modify-write control Module select inputs (used to address separate modules in a multi-module system)

## Standard output signals

Data output  
Unit available signal (memory busy)  
Data available signal  
End of cycle signal

## DC power requirement

Voltage	Regulation	Current (Max)
-15 VDC	±3%	7.2 amps (20 bits)
+5 VDC	±5%	4.5 amperes source

No temperature compensation of either voltage is necessary.

## Weight

4.0 lb.

## Dimensions

8.0 inches (203.2 mm) high  
10.0 inches (254.0 mm) deep  
2.0 inches (51 mm) wide  
(2.125 inches with optional metal cover)

## Operating Environment

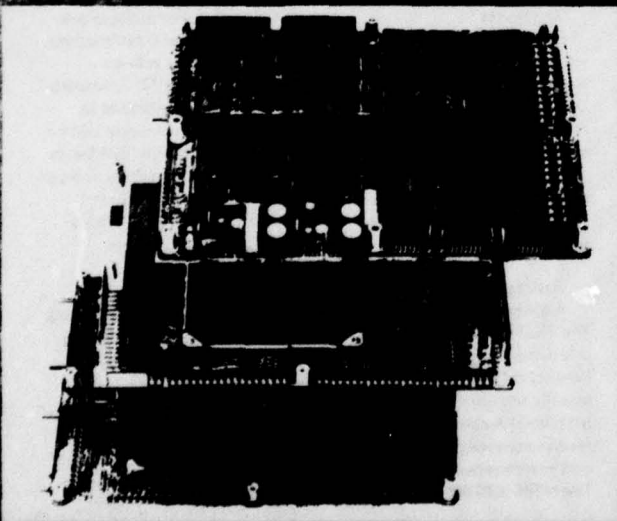
0°C to 55°C ambient temperature  
Up to 90% relative humidity with no condensation

## Non-operating environment

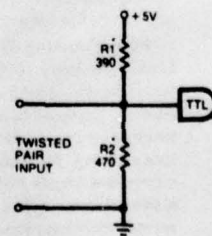
-55°C to +85°C ambient temperature  
Up to 95% relative humidity with no condensation

## Available options

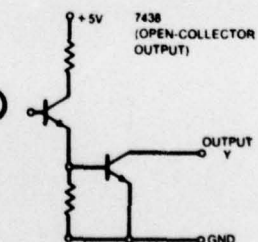
Byte control (2 bytes maximum)  
Zone control (2 zones maximum)  
External logic clear  
(Internal logic reset to ready)  
External memory register reset  
(Output lines at high logic state)  
External memory register transfer  
(For byte or zone control)  
Metal extractor handle  
Metal covers



## Typical Input Receiver



## Typical Output Driver



\*R1 and R2 will be as shown unless otherwise specified.

Litho in U.S.A. C-341 11/72

## 1800 SERIES

### AMPEX CORE MEMORY SYSTEMS USING 1800 SERIES MODULES

#### Tailored to your needs

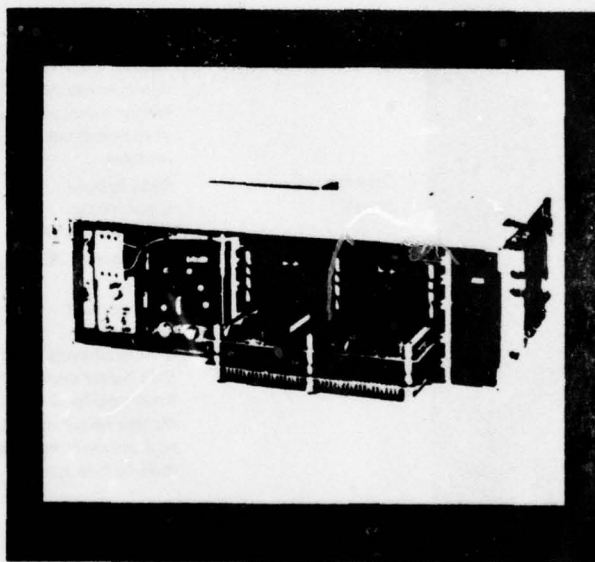
Complete Ampex 1800 Series core memory systems are designed to provide exactly the configurations and capacities you need for specialized OEM systems—at off-the-shelf prices. There are standard configurations which accommodate from two to eight memory modules. Any desired combination of standard or special interfaces, power supplies, testers, or blowers can be specified. System capacity extends all the way to 65,536 18-bit words. Word size is completely flexible—9, 12, 18 bits or longer if you choose. Access times are 230, 250, or 340 nanoseconds, and cycle times are 600, 650 or 850 nanoseconds, depending on the model you select. (Detailed performance and specification data on 1800 Series core memories is contained in individual Ampex product sheets on the following models: 1860, 1865, 1885, and the ruggedized 1800M Series.)

#### Lower design costs

You get a customized memory system—ready to plug in—for only a little more than module prices. You save even more money and time because your available design manpower can devote more effort to other portions of the system.

#### Higher packing density

Each of the basic 1800 Series memory configurations is carefully designed to provide maximum compactness and space-saving. You can build a complete Ampex memory system into your own system without sacrificing space required for other important system functions.



#### Standard or special interfaces

There are no interface problems when building the 1800 Series into your system. A standard interface is included, and space is provided in the memory card cage for any special interface you may require. If you wish, we also can supply special interface cards designed to your specification.

#### Fast, reliable, and expandable

The 1800 system is more than a fast, modular, building block memory customized to your specific requirements. It also has traditional Ampex reliability, full temperature range performance, and interchangeability. The MTBF is 10,000 hours, with

an operating range from 0°C to 55°C. For applications requiring a ruggedized memory, the 1800M Series with an extended 0°C to 70°C temperature range and resistance to shock, vibration and dust can be specified. All Ampex 1800 Series memories are completely uniform from module-to-module and can be interchanged within a single system or between different systems.

#### Optional subsystems

You can select as many or as few subsystems as you need. These include 115V or 220V blower assemblies, one or two 115V or 220V power supplies, and an on-line tester which can completely check-out total system operation. Standard connectors are supplied with all configurations.

## AMPEX

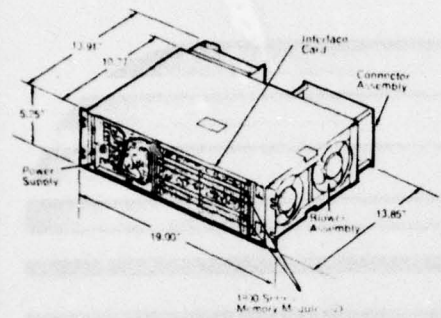
Ampex Computer Products Corporation  
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Marina del Rey, California 90291  
A subsidiary of Ampex Corporation



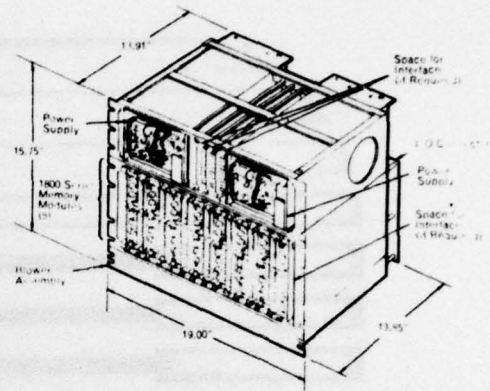
1800

# **AMPEX**

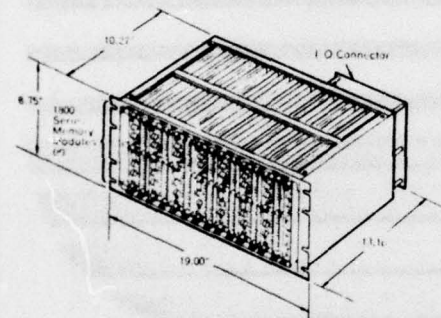
Amplex Computer Products Corporation  
13031 West Jefferson Boulevard  
Marina del Rey, California 90291  
A subsidiary of Ampex Corporation



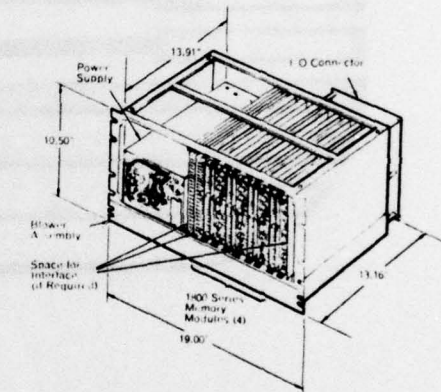
Two module configuration with interface card, power supply, connector assembly, and blower assembly.



Eight module configuration with two power supplies, blower assembly, I/O connector, and space for interface.

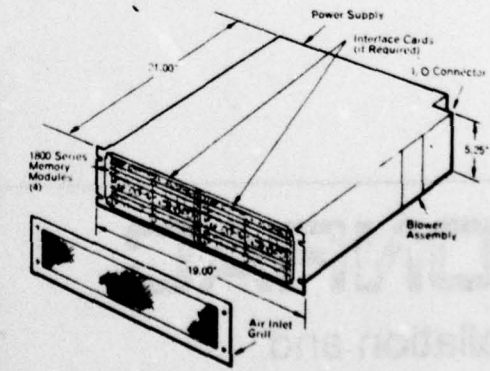
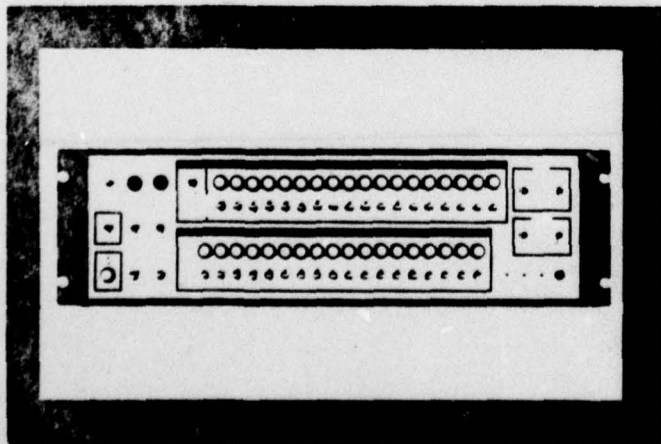


Eight module configuration with I/O connector, and space for interface.



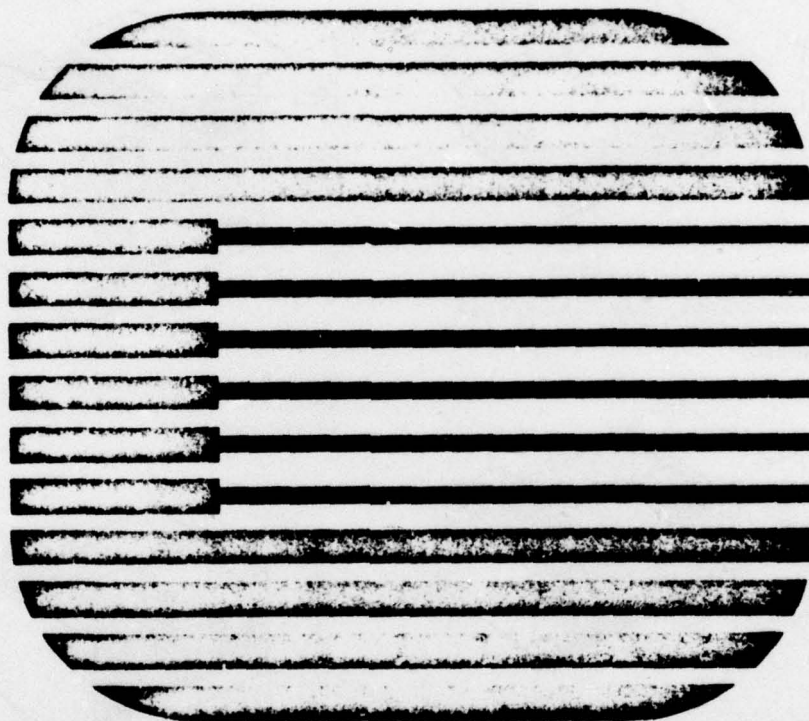
Four module configuration with power supply, blower assembly, I/O connector, and space for interface.

An optional on-line tester capable of completely checking-out total system operation is available with most 1800 Series module configurations. Optional 115V or 220V power supplies also can be selected, as well as optional 115V or 220V blower assemblies. All configurations have standard connectors.



Four module configuration with power supply, blower assembly, I/O connector, air inlet grill, and space for interface.

Litho in U.S.A. C-330 11/72



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# CONRAC

Installation and  
Operating Instructions

Color Television Monitor  
Model 5111

## GENERAL DESCRIPTION

### FEATURES

- \*Preset controls for contrast, brightness, and chroma
- \*Continuously variable aperture correction
- \*Negative black matrix shadow mask CRT
- \*Solid-state circuitry
- \*All setup controls from accessible pull-out drawer
- \*Advanced mechanical design assures structural integrity in all mounting configurations

### DESCRIPTIVE INFORMATION

The advanced design of the electronic circuitry in the 5100 Series is such that the CRT itself becomes the limiting factor in performance. A keyed backporch clamp maintains true black level when operating with either composite or non-composite video. New operator conveniences include the addition of preset controls on all versions for contrast, brightness, chroma and phase.

All secondary controls and adjustments are located in a pull-out drawer below the picture tube. This location provides maximum operator convenience, prevents unauthorized tampering and gives the monitor a clean, eye-pleasing appearance.

The chassis is arrayed in "U" configuration, permitting physical separation of power supply deflection from video amplifier/decoder circuit stages. Modular circuit boards and power supplies are interconnected by a quick-disconnect wiring harness, thus simplifying maintenance procedures.

External packaging is compatible with the most up-to-date installations and employs front and back frames. Aluminum extrusions, running from front to

back at each side, support full-length recessed carrying handles. Sheet metal covers, above and below the extrusions, complete the package.

### APPLICATION

The 5100 Series 19- and 25-inch television monitors are especially useful for group viewing in auditoriums, classrooms, lecture halls, industrial training areas, hospital paging systems, preview rooms, and other audience viewing applications. Rigid mechanical construction throughout assures structural integrity and protects all components. This is of particular importance for applications where monitors must be moved from location to location or hung from ceiling, wall or floor stand.

All units comply with U.S. Department of Health, Education and Welfare X-Radiation Safety Rules, 21 CFR, Subchapter J, applicable at time of manufacture.

### PRODUCT IDENTIFICATION

First character — Identifies the Series (5)

Second character — Identifies the significant update level (1)

Third character — Identifies the option package (1 = Standard Package)

Fourth character — Identifies the color decoder standard (0 = Not Used; 1 = RGB; 2 = NTSC; 3 = PAL B; 4 = PAL M; 5 = SECAM 50; 6 = SECAM 60)

Fifth character — Identifies mechanical configuration (C = Cabinet; N = Naked, or Chassis; RS = Rack mount with slides; Y = Yoke, or Bail Mount)

Final characters — Identify the size of the CRT

## TECHNICAL SUMMARY

### ELECTRICAL SPECIFICATIONS

<b>Input Power</b>	<b>Voltage:</b>	100V $\pm$ 10%, 50/60Hz 120V $\pm$ 10%, 50/60Hz 220V $\pm$ 10%, 50/60Hz 240V $\pm$ 10%, 50/60Hz
	<b>Power:</b>	125 watts, nominal
<b>Input Signals</b>	<b>Power</b>	
	<b>Connection:</b>	Captive 6-foot cord with three-prong connector plug
	<b>Composite:</b>	Loop-through or switchable to internal 75 $\Omega$ termination. 1.0V peak-to-peak, nominal (0.35V to 2.0V) Sync is negative.
	<b>Non-Composite:</b>	0.7V peak-to-peak, nominal (0.25V to 1.4V), Black negative.
<b>Video Input</b>	<b>Return Loss:</b>	Greater than 40dB
<b>Video Response</b>		Monochrome signal applied $\pm$ 1dB to 5 MHz
<b>Differential Gain</b>		Less than 5% for luminance of 0fL to 20fL.
<b>Aperture Correction</b>		A continuously adjustable front panel control provides up to 6dB boost at 3.2MHz.
<b>Decoder Accuracy</b>		Decoder error less than 1.5°.
<b>Linearity and Geometry</b>		No point on raster deviates from its proper position by more than 2% of raster height.
<b>Convergence</b>		On the 19-inch models, does not deviate more than .040" or 1.02mm (.051" or 1.30mm on 25" models) from picture height in a centrally located area bounded by a circle. The diameter of this circle is equal to the picture height. Elsewhere, the deviation does not exceed .080" or 2.04mm (.100" or 2.54mm on 25-inch models).
<b>Color Temperature</b>		The range of RGB gain adjustments is sufficient to permit setting white color temperature to 6500°K (factory setting) or 9300°K.
<b>Color Temperature Accuracy</b>		Color temperature of white does not change by more than one MPCD unit between monochrome and color input signals.
<b>Interlace</b>		Better than 90%.
<b>Raster Size Regulation</b>		Less than 1% change, 0% to 100% APL (Average Picture Level) at peak 20fL luminance.
<b>Black Level Stability</b>		DC restorer maintains black level shift less than 1% of peak luminance from 10% to 90% APL.
<b>Discernible Shades of Gray</b>		10 minimum.
<b>Vertical Retrace Time</b>		1000 $\mu$ sec nominal.
<b>Horizontal Retrace Time</b>		10 $\mu$ sec nominal.
<b>Radiation</b>		All units comply with the U.S. Department of Health, Education and Welfare X-Radiation Safety Rules, 21 CFR, Subchapter J, applicable at time of manufacture.
<b>Ambient Temperature and Humidity</b>		10° to 50°C operating temperature; 10% to 90% relative humidity; no condensation.

## MECHANICAL CONFIGURATION

### Construction

The chassis, which is constructed of heavy-gauge aluminum, is arrayed in "U" configuration, permitting physical separation of power supply deflection from video amplifier/decoder circuit stages. Modular circuit boards and power supplies are interconnected by quick-disconnect wiring harnesses, simplifying maintenance procedures.

External packaging is compatible with the most up-to-date installations.

### Frames

Aluminum extrusions, running from front to back at each side, form full-length recessed carrying handles. Sheet metal covers, above and below the extrusions, complete the package. These are easily removable for maintenance purposes. Conversion from cabinet to rack mounting is accomplished by removing the sheet metal covers and side extrusions and installing rack rails. The CRT is finished in black and all exposed knobs and switches are dull finish plated for minimum viewer distraction.

### Weight

MODEL	NET WEIGHTS	SHIPPING WEIGHTS
5100C19	99 lbs. 44.9 kilos	112 lbs. 50.8 kilos
5100RS19	98 lbs. 44.5 kilos	111 lbs. 50.4 kilos
5100Y19	99 lbs. 44.9 kilos	112 lbs. 50.8 kilos
5100C25	146 lbs. 66.2 kilos	158 lbs. 71.7 kilos
5100Y25	146 lbs. 66.2 kilos	158 lbs. 71.7 kilos



**General DataComm Industries, Inc.**

131 DANBURY ROAD, WILTON, CONNECTICUT 06897, TELEPHONE (203) 762-0711

## GDC 201-9(R) LSI SYNCHRONOUS MODEM

### FEATURES:

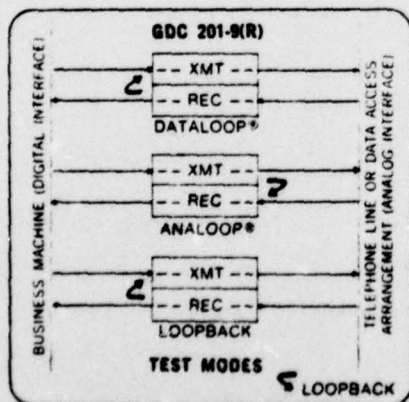
- LSI Technology
- 2000 or 2400 bps Operation
- Remote Analoop® and Dataloop® Addressable Diagnostics for Point-to-Point and Multipoint Applications
- Dial or Dedicated, Two-Wire or Four-Wire Operation
- Stand Alone or Rack Mount
- Alternate Voice
- Secondary Channel, Forward or Reverse Operation
- WECC 201A or 201B Compatible
- Local Analoop® and Loopback Self-Test

### APPLICATION

The General DataComm 201-9(R) is a synchronous 2000 or 2400 bps modem designed to operate over unconditioned 2- or 4-wire type 3002 private lines or over the DDD switched network via the Manual Data Coupler CDT (10C0A). The GDC 201-9(R) is fully compatible with WECC 201A (2000 bps) or 201B (2400 bps) data sets. Standard features include automatic fast sync, clear to send delay, carrier detect, external/internal transmitter timing and MARK hold on receive data when carrier is lost.

Available for rack mounting (201-9R) at the CPU site or as a stand alone, single channel subset (201-9) for remote locations, the General DataComm 201-9 (R) LSI modem incorporates unique diagnostic functions which permit local verification of modem and system operation without the need for special tools or test equipment.

The unit is also available equipped with a diagnostic control card which permits the use of remote addressable diagnostics on a multipoint system. Simple front panel diagnostic switch controls and lighted indicators on both configurations provide complete performance assurance at your installation.



### UNIQUE DIAGNOSTICS

Unsurpassed local and remote diagnostics inherent in the GDC 201-9(R) provide for rapid trouble shooting within the entire communications system. The remote Dataloop® diagnostic feature of the 201-9(R) provides remote loopback of the modem on the digital side in either point-to-point or multipoint systems. The unique Analoop® diagnostic command will loop the local or remote modem back on itself on the analog side, as well as the private line's receive side to the transmit side.

In multipoint applications an Address Generator is provided which generates a unique address associated with each remote modem. Therefore, by use of the Analoop® and Dataloop® diagnostics, each individual remote location can be analyzed with respect to terminal, modem, or private line failure. This concept of Addressable Diagnostics allows a

## GDC 201-9(R) LSI SYNCHRONOUS MODEM

user to isolate faults in a matter of minutes.

In addition to the remote Addressable Diagnostic features, there are others which aid in diagnosing system problems. These include a Test Generator/Recognizer and an Alternate Voice facility. The Alternate Voice facility includes Ring Signal transmission circuitry, Ring Signal indicator, and interface for the GDC auxiliary telephone set. The auxiliary telephone set provides alternate voice capability and also monitoring capability without interfering with data transmission.

### SPECIFICATIONS

**Operating Modes:** Simplex or half-duplex on two-wire lines and half or full-duplex on four-wire lines; strap selectable between two-wire and four-wire operation.

**Modulation:** Differential phase shift keyed 1800 Hz carrier, four phase. Transmit signal includes full bandwidth required for WECO 201 compatibility.

**Operating Speeds:** 2000 or 2400 bits per second, serial, synchronous on DDD or unconditioned 3002 lines.

**Carrier Detect Response:** Operate Time  $10 \pm 1$  ms  
Release Time  $8 \pm 1$  ms

**Transmit Level:** +2 to -10 dbm, adjustable via calibrated potentiometer.

**Receive Level:** Nominal -10 to -40 dbm, adjustable via calibrated potentiometer. Dynamic range  $\pm 15$  db around nominal.

**Transmit Clock:** (strap selectable)  
Internal:  
2000 or 2400 Hz  $\pm 0.01\%$  square wave  
External:  
2000 or 2400 Hz  $\pm 0.01\%$  square wave  
50  $\pm 5\%$  duty cycle

**Receive Clock:** 2000 or 2400 Hz square wave synchronized with incoming data. Receive data transition coincides with positive edges of clock.

**Fast Sync:** Provides for externally imposing Fast Sync where time between messages is less than 10 ms.

**Equalizer:** Statistical equalizer provides equalization of most commonly encountered telephone line amplitude and delay characteristics.

**EIA RS-232B/C Compatible:**

Input:  
SPACE (or ON) +3 to +25 V  
MARK (or OFF) -3 to -25 V  
Output:  
SPACE (or ON) +11 to  $\pm 1$  V  
MARK (or OFF) -10  $\pm 1$  V

**Power Supply Requirements:** AC Power: 115 V, 60 Hz  
15 Watts

**Operating Temp:** 0 to 70°C

**Storage Temp:** -20°C to 85°C

**Rel. Humidity:** 5% to 95%

### ORDERING INFORMATION

Specify:

**Configuration**

List 1 2000 bps Operation

→ List 2 2400 bps Operation

**Options**

List 3 Remote Diagnostics

List 4 Single Channel Address Generator/Telephone

List 5 Rack Mount Address Generator/Telephone for up to 12 modems

List 6 Remote Telephone for Alternate Voice

List 7 Reverse Channel (75/110 baud)

List 8 Secondary Channel

For additional information, contact:  
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General DataComm Industries, Inc.  
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9DPL5M

**MODEM JUMPER POSITIONS AND CONTROL SETTINGS  
FOR DIRECT 4-WIRE INTERCONNECTION**

<u>CARD</u>	<u>Position</u>	<u>Jumper or Control Name</u>	<u>Position</u>
201 RCV	Top	CCITT	B
		SCRAMBLE	OUT
		FST SYNC	OUT
201 T/R	Center	SCRAMBLE	OUT
		CAR	NORM
		XMT	VAR
		XMT POT	-10 (dBm)
		A/B	B
		TMG	INT
		RCV	VAR
		RCV POT	-10 (dBm)
		EQ	OUT
		2W/4W	4W
		2W/4W	4W
		CB	8.5
		CB/8.5/175	8.5/175
		SQ	100
		XMT/RCV	4W

## 1. SPECIFICATIONS

The INFOTON VISTAR/GT is a stand-alone alphanumeric display terminal for use in data entry and retrieval systems where a highly flexible interaction between man and machine is desired. The VISTAR/GT incorporates such important standard features as conversational mode, and an Infotone which operates on the bell code. Complete specifications are listed in INFOTON Document No. 02421.

### 1.1 BASIC SYSTEM

Power	Domestic: 100 watts, 105-130 volts; 60 Hz Export: 100 watts; 105-130, 210-260 volts; 50 Hz
Temperature	Operating: 0° to 50°C Storage: -30° to 70°C
Humidity	0% to 95% non-condensing
Dimensions	13 inches high, 19 5/8 inches wide, 23 3/4 inches deep
Weight	35 pounds
Screen Size	12 inch diagonal
Display Size	8 1/2 inches wide, 6 inches high
Characters/Line	80
Lines	24
Line Spacing	0.45 character height
Character Format	5 x 7 dot matrix
Character Spacing	0.4 character width
Character Size	0.08 x 0.19 inch nominal
Character Repertoire	64 ASCII
Refresh Rate	Domestic: 60 times a second Export: 50/60 times a second
Cursor	Non-destructive blinking underscore
Transmit Data	Character by character as entered by the keyboard.

### 1.2 STANDARD INTERFACE

The Asynchronous Serial Interface is a multi-purpose serial data interface which provides maximum flexibility in operator switch selectable data rates, and operation modes that can be applied to allow operation under a wide variety of serial data input and output situations. A panel at the rear of the display contains switches and connectors that allow the operator to match both the standard EIA RS232C voltage interface and the Teletype\* compatible 20/60 mA current loop interface for serial communications and computer interfaces.

\*Registered Trade Mark of Teletype Corporation

The operator selectable functions include the following:

1. Eleven Receive data rates — 75, 110, 150, 300, 600, 1200, 1800, 2400, 4800, 7200, and 9600 bits per second
2. An external TTL clock input
3. Full or Half Duplex
4. Ten or eleven bit code selection (one or two stop bits)
5. Odd, Even, or Mark Parity
6. 20 or 60 mA Teletype\* compatible current loop interface
7. EIA RS232C interface - Interfaces to Bell system Type 103A, 103F, 202C, 202D modems or equivalents

\*Registered Trade Mark of Teletype Corporation



**MEASUREMENT SYSTEMS, INCORPORATED**

## **TRACKBALL MODEL 628**

*for*

**GRAPHIC DISPLAYS**

**AIR TRAFFIC CONTROL**

**RADAR CURSORS**

**MACHINE TOOL CONTROL**



A small size trackball built to meet rugged environmental requirements is now available from stock in sample quantities.

### **EASY TO OPERATE**

The Model 628 trackball is a fast and accurate 2 axis manual positioning device requiring a minimum amount of operator training and skill. Electrical signals proportional to magnitude and direction are resolved into X and Y components as the ball is rotated by the operator. Typically, bi-directional optical encoders are used that produce TTL pulses on an "up-count" or a "down-count" line.

### **DESIGN FEATURES**

A 3 inch dia. ball in a 4.5 inch square package only 2.25 deep make this product a real space saver suitable for all but the most compact console designs. A drip-proof seal is standard on all models.

### **SMOOTH MOTION**

Unique bearing and pick-off wheel designs provide this unit with the lowest operating force available. Tangential force required to move the ball in any direction is less than 2 ounces. Additional friction can be readily added to hold the ball from turning for turbulent environment applications.

### **MODEL 628 square waves**

Uses long life optical shaft encoders that produce square waves in quadrature as the ball is rotated. The standard rate is 300 complete cycles per rotation of the ball. Output levels are TTL compatible, positive 5 volt. Other pulse rates available.

### **MODEL 628-1 potentiometer**

Features multi-turn potentiometers that rotate full range for 3 turns of the ball. Resolution is .03% for standard 10k ohm potentiometers. Other resistance values are available.

### **MODEL 628-4 TTL pulses**

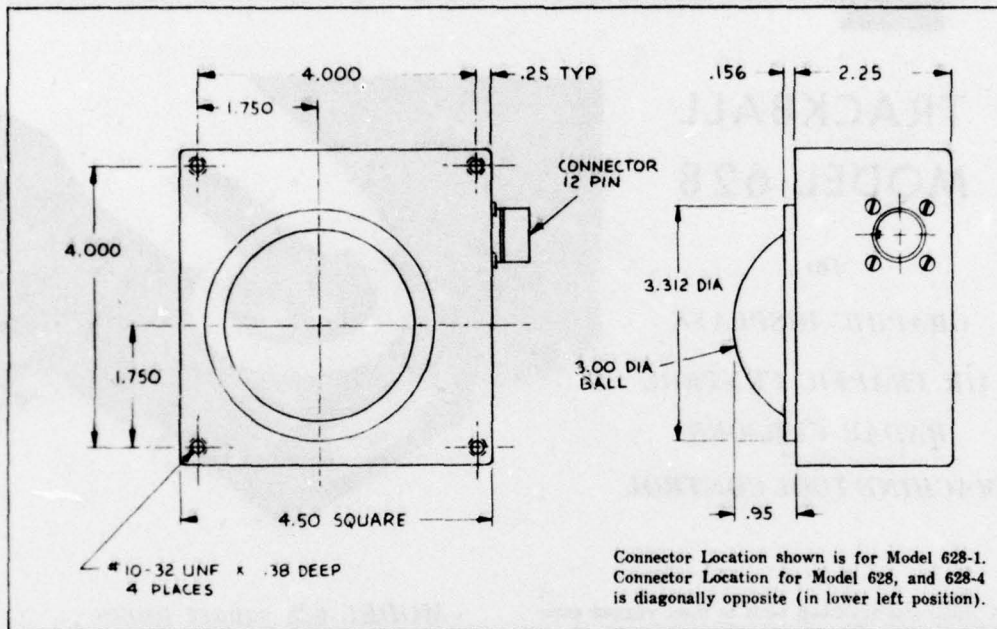
Identical to the 628 described above but with an additional logic circuit built into the package. Output becomes TTL pulses on an "up-count" line or a "down-count" line depending upon direction of rotation.

REPRESENTED BY  
TEKDATA

DEC. 73

**MEASUREMENT SYSTEMS, INC. . . . 523 WEST AVENUE, NORWALK, CONN. . . . 203 838-5561.**

## MODEL 628 TRACKBALL



### SPECIFICATIONS

Weight .....	Less than 2 lbs
Tracking Force .....	Nom 1.5 oz, Max 2.0 oz
Housing .....	Aluminum Casting, Black
Environmental Seal .....	Drip Proof MIL-STD-108
MTBF .....	25,000 Hours
Power Requirements, Optical .....	+ 5vdc, 400ma
Connector .....	Amphenol 67-02E-14-12P
Counts per Revolution .....	300 Standard, other counts available

MODEL NO.	RESOLVER	OUTPUT, EACH AXIS
628	Optical Encoders	Square Waves in Quadrature +5V
628-1	Multi-turn Potentiometer	10k ohm, 1 watt, .03%, 3 turns full range
628-4	Optical Encoders	TTL Pulses on "Up" or "Down" line

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

MEASUREMENT SYSTEMS, INC. . . . 523 WEST AVENUE, NORWALK, CONN. . . . 203 838-8561.



## GENERAL PURPOSE, ANALOG-TO-DIGITAL CONVERTERS

### ADC-MA SERIES

#### FEATURES

- ▶ 10 & 12 Bit Resolution
- ▶ Selectable Input Ranges
- ▶ 20 & 40  $\mu$ sec. Conversion Times
- ▶ Unipolar or Bipolar Operation
- ▶ Input Buffer Option
- ▶ Parallel & Serial Outputs

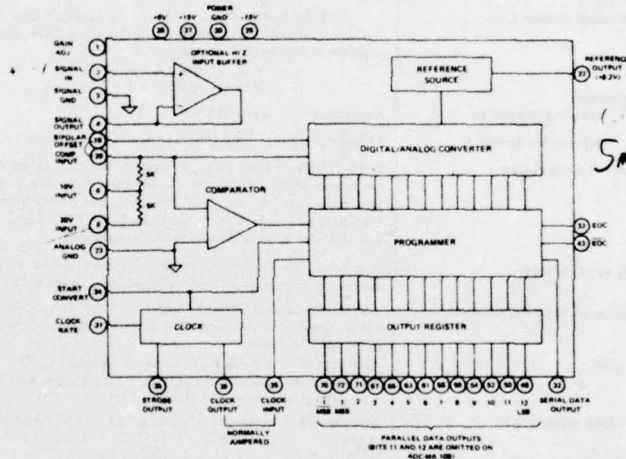
#### GENERAL DESCRIPTION

The ADC-MA series A/D converters consist of 10 and 12 bit resolution models with 20 or 40 microsecond conversion times. These units feature high performance and versatility at a low price.

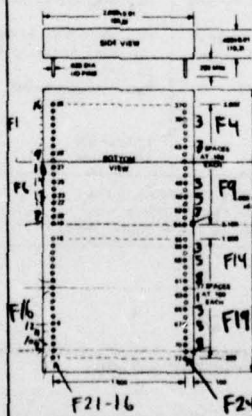
The exceptional versatility of the ADC-MA series is seen in the following features. Single-ended input voltage ranges of 0 to +5V, 0 to +10V,  $\pm 5$ V, and  $\pm 10$ V are pin selectable by the user. In addition, an internal high input impedance buffer amplifier is available as an option. This amplifier gives an input impedance of 1000 megohms on all voltage ranges. Without the amplifier the input impedances are 2.5K, 5K, and 10K ohms on 5V, 10V, and 20V full scale ranges respectively. Digital output data is available in either parallel form or serial NRZ format with synchronizing strobe pulses. Serial data is straight binary for unipolar operation and offset binary for bipolar operation. Parallel data is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. The ADC-MA units can operate either internally or externally clocked. In addition, the internal clock rate can be decreased by use of an external capacitor.

The ADC-MA series uses the successive approximation technique to achieve excellent linearity, speed, and stability. Temperature coefficient is held to  $\pm 30$ ppm/ $^{\circ}$ C for gain and  $\pm 5$ ppm/ $^{\circ}$ C for offset in unipolar operation. Tight temperature tracking of the weighted current sources results in monotonic operation with no missing codes over the 0 $^{\circ}$ C to 70 $^{\circ}$ C temperature operating range.

These converters are encapsulated in a 4 x 2 x 0.4 inch module with DIP compatible .100" pin spacing. Input power requirements are  $\pm 15$ VDC and  $\pm 5$ VDC and are available from Datel's line of modular power supplies. All digital inputs and outputs are DTL/TTL compatible.



#### MECHANICAL DIMENSIONS INCHES (MM)



NOTE: Open dots designate omitted pins. Pins 48 and 80 are omitted on 10 bit versions and pin 82 is the LSB. Pin position tolerance is  $\pm 0.008$ " from datum, non-accumulative.

#### INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Gain Adjust	35	Clock Input
2	Signal Input	36	Clock Output
3	Signal Gnd	39	Strobe Output
4	Signal Output	43	E.O.C. (Status)
5	20 V. Input	48	Bit 12 Out (LSB)
6	10 V. Input	50	Bit 11 Out
19	Bipolar Offset	52	Bit 10 Out
20	Comparator In.	54	Bit 9 Out
22	Reference Out	56	Bit 8 Out
23	Analog Gnd	58	Bit 7 Out
25	-15V Pwr In	61	Bit 6 Out
27	+15V Pwr In	63	Bit 5 Out
28	+5V Pwr In	65	Bit 4 Out
30	Power Gnd	67	Bit 3 Out
31	Clock Rate	70	Bit 2 Out (MSB)
32	Serial Output	71	Bit 1 Out
33	E.O.C. (Status)	72	Bit 0 Out (MSB)
34	Start Convert		

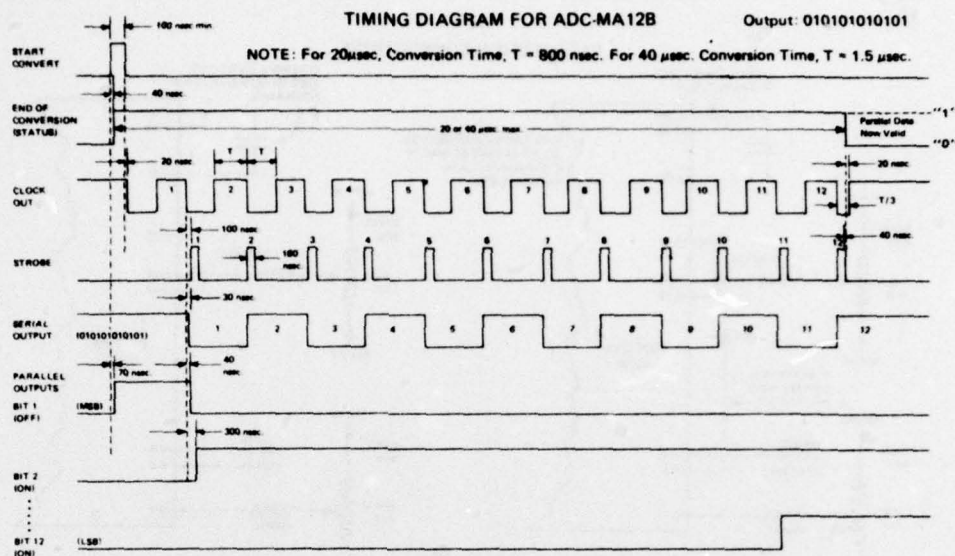
SPECIFICATIONS (typical @ 25°C unless otherwise noted)		
	ADC-MA120	ADC-MA122
<b>INPUTS</b>		
Analog Input Range . . . . .	0 to +5V FS, 0 to +10V FS, ±5V FS, ±10V FS ±15V without damage to unit	
Input Overvoltage . . . . .		
Input Impedance . . . . .		
0 to +5V FS Range . . . . .	2.5K ohms	2.5K ohms
±5V and 0 to +10V FS Range . . . . .	5K ohms	5K ohms
±10V FS Range . . . . .	10K ohms	10K ohms
With Optional Input Buffer . . . . .	1000 Megohms	1000 Megohms
Start of Conversion . . . . .	+2V min. to +5.5V max. positive pulse, DC coupled, with duration of 100 nsec. min. Rise and fall times 500 nsec. max. Three TTL loads. Logic "1" resets converter. Transition to logic "0" initiates conversion.	
Clock Input . . . . .	Must be connected to Clock Output to use internal clock. Clock Input can also be used with an external clock.	
Clock Rate . . . . .	Rate is internally set to give maximum conversion rate of 20 or 40 $\mu$ sec. per conversion. This time may be increased with an external capacitor connected between pin 31 (Clock Rate) and pin 36 (Clock Out). See conversion time formulas.	
<b>OUTPUTS</b>		
Parallel Output Data . . . . .	10 Lines of data Data is held until next conversion command. Each output is capable of driving 5 TTL loads. V out (Logic "0") < +0.4V V out (Logic "1") > +2.4V	12 Lines of data
Coding . . . . .		
Unipolar Operation . . . . .	Straight Binary, positive true.	
Bipolar Operation . . . . .	Offset Binary or Two's Complement, positive true.	
Serial Output Data . . . . .	NRZ (nonreturn to zero) successive decision pulse output generated during conversion with MSB first. Serial data is straight binary for unipolar operation and offset binary for bipolar operation. Output will drive 10 TTL loads. Two's complement is not available with serial output.	
Strobe Output . . . . .	Available for serial data synchronization. Serial output is usable on strobe pulse leading edges. Will drive 9 TTL loads.	
EOC (End of Conversion) . . . . .	Conversion status output. Logic "0" for conversion complete, Logic "1" during reset and conversion period. Will drive 10 TTL loads.	
EOC . . . . .	Complement of End of Conversion output. Logic "1" for conversion complete and Logic "0" during reset and conversion period. Will drive 7 TTL loads.	
Clock Output . . . . .	Internal clock pulse train output gated on during conversion time.	
Signal Output . . . . .	Output of optional internal buffer amplifier.	
<b>PERFORMANCE</b>		
Resolution . . . . .	10 Bits (one part in 1024)	12 Bits (one part in 4096)
Accuracy . . . . .	±.05% FS ±½LSB	±.012% FS ±½LSB
Linearity . . . . .	±½LSB	±½LSB
Temp. Coefficient of Gain . . . . .	±30 ppm/°C max. of Reading	±30 ppm/°C max. of Reading
Temp. Coefficient of Zero . . . . .		
Unipolar . . . . .	±5 ppm/°C max. of Range	±5 ppm/°C max. of Range
Bipolar . . . . .	±10 ppm/°C max. of Range	±10 ppm/°C max. of Range
Conversion Time, max. . . . .	20 or 40 $\mu$ sec. (depending on model)	20 or 40 $\mu$ sec. (depending on model)
Power Supply Sensitivity (tracking ±15V supplies)		
Gain . . . . .	±20 ppm/%	±20 ppm/%
Zero . . . . .	±10 ppm/%	±10 ppm/%
<b>POWER REQUIREMENT</b> (with input buffer amplifier)		
+15VDC ±0.5V @ 40mA, max. -15VDC ±0.5V @ 45mA, max. +5VDC ±0.25V @ 200mA, max.		
<b>PHYSICAL-ENVIRONMENTAL</b>		
Operating Temperature Range . . . . .	0°C to 70°C	
Storage Temperature Range . . . . .	-55°C to +85°C	
Relative Humidity . . . . .	Up to 100% non-condensing	
Case Size . . . . .	4" x 2" x 0.4"	
Case Material . . . . .	Black Diallyl Phthalate per MIL-M-14, epoxy encapsulated.	
Pins . . . . .	.020" round, gold plated, .250" long min.	
Weight . . . . .	8 oz. (227 grams)	
Mating Sockets (optional) . . . . .	DILS-2, 4 required.	

## TECHNICAL NOTES

The ADC-MA series contains an internal clock which is set to the maximum conversion rate. This rate may be decreased by connecting an external capacitor between pins 31 and 36. The approximate capacitor value to achieve the desired conversion time is shown in the table at the bottom of the next page. The longer conversion time obtained in this manner does not improve accuracy but it does permit compatibility or synchronization with interfacing equipment for many applications. To use the internal clock a jumper must be connected between pins 35 and 36. For external clocking, which may be desirable in some applications, the jumper is removed and the external clock applied to pin 35. Use a symmetrical 0 to +5V square wave with a minimum 3.0  $\mu$ sec. period for the 40  $\mu$ sec. converters and a minimum 1.6  $\mu$ sec. period for the 20  $\mu$ sec. converters. The Start Convert pulse should have a minimum 100 nsec. width and should not be made too long since clocking begins on the falling edge of this pulse and, therefore, its width is part of the total conversion time.

Analog inputs are connected to pin 6 for 10V ranges and pin 5 for the 20V range when the input buffer amplifier is not used. The input impedances in these cases are 5K ohms and 10K ohms respectively. For the 0 to 5V range, pin 5 is connected to pin 20, thus paralleling the two internal 5K resistors to give a 2.5K ohm input impedance at pin 6.

The end of conversion or status pulse is available at pin 33 and its complement EOC is available at pin 43. Normally the EOC output is used to control the mode of the input sample and hold. Serial output data is available at pin 32 in straight binary code for unipolar operation or offset binary for bipolar operation. Nonreturn to zero (NRZ) format is used and the data is valid at the leading edge of the strobe pulse. Parallel data output is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. Two's complement is obtained by using the complemented MSB output at pin 70.



#### OUTPUT DIGITAL CODING, ADC-MA SERIES

ADC-MA12B (12 BITS)

UNIPOLAR INPUT RANGE		STRAIGHT BINARY MSB    LSB	BIPOLAR INPUT RANGE		OFFSET BINARY MSB    LSB	TWO'S COMPLEMENT MSB    LSB
0 TO +10V FS	0 TO +5V FS		±10V FS	±5V FS		
+9.9978	+4.9988	111111111111	+9.9951	+4.9978	111111111111	011111111111
+8.7500	+4.3750	111000000000	+7.5000	+3.7500	111000000000	011000000000
+7.5000	+3.7500	110000000000	+5.0000	+2.5000	110000000000	010000000000
+5.0000	+2.5000	100000000000	0.0000	0.0000	100000000000	000000000000
+2.5000	+1.2500	010000000000	-5.0000	-2.5000	010000000000	110000000000
+1.2500	+0.6250	001000000000	-7.5000	-3.7500	001000000000	101000000000
+0.0024	+0.0012	000000000001	-9.9951	-4.9978	000000000001	100000000001
0.0000	0.0000	000000000000	-10.0000	-5.0000	000000000000	100000000000

ADC-MA10B (10 BITS)

UNIPOLAR INPUT RANGE		STRAIGHT BINARY MSB    LSB	BIPOLAR INPUT RANGE		OFFSET BINARY MSB    LSB	TWO'S COMPLEMENT MSB    LSB
0 TO +10V FS	0 TO +5V FS		±10V FS	±5V FS		
+9.9902	+4.9951	1111111111	+9.9805	+4.9902	1111111111	0111111111
+8.7500	+4.3750	1110000000	+7.5000	+3.7500	1110000000	0110000000
+7.5000	+3.7500	1100000000	+5.0000	+2.5000	1100000000	0100000000
+5.0000	+2.5000	1000000000	0.0000	0.0000	1000000000	0000000000
+2.5000	+1.2500	0100000000	-5.0000	-2.5000	0100000000	1100000000
+1.2500	+0.6250	0010000000	-7.5000	-3.7500	0010000000	1010000000
+0.0088	+0.0044	0000000001	-9.9805	-4.9902	0000000001	1000000001
0.0000	0.0000	0000000000	-10.0000	-5.0000	0000000000	1000000000

#### EXTERNAL PIN CONNECTIONS

INPUT RANGE (FS)	BUFFER OPTION	INPUT TO PIN	JUMPER PIN 4 TO	JUMPER PIN 20 TO	JUMPER PIN 19 TO
0 TO +10V	WITHOUT	6	—	—	23
	WITH	2	6	—	23
±5V	WITHOUT	6	—	—	20
	WITH	2	6	—	20
±10V	WITHOUT	6	—	—	20
	WITH	2	5	—	20
0 TO +5V	WITHOUT	6	—	5	28
	WITH	2	6	5	23

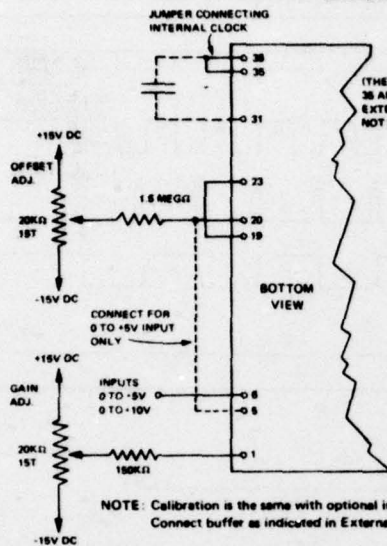
#### CONVERSION TIME USING EXTERNAL CAPACITOR

The external capacitor is connected between pins 31 and 36. Conversion time in the table is in microseconds and capacitor value is in picofarads.

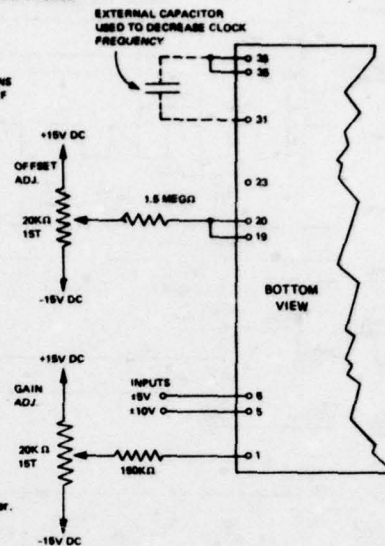
Conversion Time Formula (approx.)		
Conv. Time*	ADC-MA10B	ADC-MA12B
20 μsec.	C = 68(T-20μsec.)	C = 50 (T-20μsec.)
40 μsec.	C = 65(T-40μsec.)	C = 55(T-40μsec.)

\* Maximum internal conversion rate when no external capacitor is used.

## CALIBRATION CONNECTIONS



UNIPOLAR OPERATION (WITHOUT BUFFER)



BIPOLAR OPERATION (WITHOUT BUFFER)

NOTE: Calibration is the same with optional input buffer amplifier. Connect buffer as indicated in External Pin Connections.

## CALIBRATION PROCEDURE

Gain and offset adjustments are accomplished as shown in the above diagram using the Calibration Table. The trimming potentiometers used should be 15 turn 100ppm/°C temperature coefficient cermet type units and are available from Datal Systems at \$3.00 each. A pulse generator should be adjusted to give +5 volt pulses with 100 nsec. minimum duration and a spacing equal to or larger than the specified maximum conversion time (20 or 40 usec.). This generator should be connected to the "Start Convert" input. A precision voltage reference source should be connected to the selected analog input terminal.

**Offset Adjustment:** For unipolar operation set the output of the voltage reference source to zero plus 1/2 LSB. The value is shown in the Calibration Table. Adjust the offset trimming potentiometer until the LSB output flickers equally between logic "0" and logic "1". (Output between 000...000 and 000...001). For bipolar operation set the voltage reference source to minus full scale plus 1/2 LSB and make the same adjustment.

**Gain Adjustment:** Adjust the output of the voltage reference source to full scale minus 1 1/2 LSB. This value is also shown in the Calibration Table. Adjust gain trimming potentiometer until LSB output flickers equally between logic "0" and logic "1". (Output between 111...110 and 111...111).

## CALIBRATION TABLE ADC-MA SERIES

INPUT RANGE	ADJUST- MENT	INPUT VOLTAGE	
		10 BIT	12 BIT
UNIPOLAR	0 TO +5V	OFFSET	2.4 mV
		GAIN	+4.9927V
	0 TO +10V	OFFSET	4.9 mV
		GAIN	+9.9854V
BIPOLAR	±5V	OFFSET	-4.9951V
		GAIN	+4.9854V
	±10V	OFFSET	-9.9902V
		GAIN	+9.9707V

## ORDERING INFORMATION

ADC-MA		
NUMBER OF BITS AND CODING	WITH OR W/O HIGH Z BUFFER	CONVERSION TIME
10B = 10 BINARY BITS 12B = 12 BINARY BITS	1 = WITH 2 = WITHOUT	A = 40µSEC B = 20µSEC

## ADC-MA10B1A PRICES (1-9)

ADC-MA10B2A .. \$ 99.00	ADC-MA12B2A .. \$129.00
ADC-MA10B2B .. \$129.00	ADC-MA12B2B .. \$149.00

For optional internal high impedance buffer amplifier add \$20.00 to price.

Mating Socket: D1LS-2, 4 required @ \$5.00 per pair  
Trimming Potentiometers: TP20K \$3.00 each (1-9)

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SYSTEMS, INC.

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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

1020 TURNPIKE STREET, CANTON, MASS. 02021 TEL (617) 828-8000 TWX 710-348-0135 TELEX 924461

8/74 BULLETIN AMA-L15408

## APPENDIX B

### READ-ONLY-MEMORY TRUTH TABLES

DRU Card, D20 Harris H PROM 1-8256-5B (32 x 8)

		PA(Y)	LA(Y)	CP	CPA3	CPA2	CPA1	CPA0		
Address		B7	B6	B5	B4	B3	B2	B1	B0	
0 (32)				H	H	H		H	H	0
1				H		H		H	H	1
2				H		H		H	H	2
3				H	H	H	H			3
4 (36)				H		H	H			4
5				H		H	H			5
6				H	H	H	H		H	6
7				H		H	H		H	7
8 (40)				H		H	H		H	8
9				H	H	H	H	H		9
10				H		H	H	H		10
11				H		H	H	H		11
12 (44)				H	H	H	H	H	H	12
13	X									13
14	X									14
15	X		H							15
16 (48)			H							16
17			H							17
18	X		H						H	18
19			H						H	19
20 (52)			H						H	20
21	X		H					H		21
22			H					H		22
23			H					H		23
24 (56)	X		H					H	H	24
25			H					H	H	25
26			H					H	H	26
27	X									27
28 (60)	X									28
29	X									29
30	X									30
31 (63)	X									31

H ≡ High ≡ Logic One ≡ Programmed  
Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

DCU Card, D20 Harris H PROM 1-8256-5B (32 x 8)

		PA(Y)	LA(Y)	CP	CPA3	CPA2	CPA1	CPA0		
Address		B7	B6	B5	B4	B3	B2	B1	B0	
0 (32				H	H	H		H	H	0
1				H		H		H	H	1
2				H		H		H	H	2
3				H	H	H	H			3
4 (36)				H		H	H			4
5				H		H	H			5
6				H	H	H	H		H	6
7				H		H	H		H	7
8 (40)				H		H	H		H	8
9				H	H	H	H	H		9
10				H		H	H	H		10
11				H		H	H	H		11
12 (44)				H	H	H	H	H	H	12
13	X									13
14	X									14
15			H		H					15
16 (48)			H							16
17			H							17
18			H		H				H	18
19			H						H	19
20 (52)			H						H	20
21			H		H			H		21
22			H					H		22
23			H					H		23
24 (56)			H		H			H	H	24
25			H					H	H	25
26			H					H	H	26
27	X									27
28 (60)	X									28
29	X									29
30	X									30
31 (63)	X									31

H ≡ High ≡ Logic One ≡ Programmed  
Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

DRU, DCU Card, C16 Harris H PROM 1-8256-5B (32 x 8)

		PA(Y)	LA(Y)	CP	CPA3	CPA2	CPA1	CPA0		
Address		B7	B6	B5	B4	B3	B2	B1	B0	
0	X								0	
1	X								1	
2				H	H				2	
3				H					3	
4				H					4	
5				H	H			H	5	
6				H				H	6	
7				H				H	7	
8				H	H			H	H	8
9				H				H	H	9
10				H				H	H	10
11				H	H		H			11
12				H			H			12
13				H			H			13
14				H	H		H		H	14
15				H			H		H	15
16				H			H		H	16
17				H	H		H	H		17
18				H			H	H		18
19				H			H	H		19
20				H	H		H	H	H	20
21				H			H	H	H	21
22				H			H	H	H	22
23				H	H	H				23
24				H		H				24
25				H		H				25
26				H	H	H			H	26
27				H		H			H	27
28				H		H			H	28
29				H	H	H		H		29
30				H		H		H		30
31				H		H		H		31

H = High = Logic One = Programmed  
Blank = Low = Logic Zero = Not Programmed

SDF Card, B15 Signetics 82S123 (32 x 8)  
 DRU Card, B20, D30

Address		01111 B7	B6	B5	WL8P B4	WL1P B3	31BG B2	4BG B1	Sync. Code B0
PT 1	LSB 0				H				H
	1								H
	2			H					H
	MSB 3				H				H
PT 2	4				H				H
	5								
	6								
	7				H				H
PT 3	8				H				H
	9								
	10								H
	11				H				
PT 4	12				H	H			H
	13								
	14								
	15	H			H	H			
PT 5	16				H				
	17								
	18								H
	19				H				
PT 6	20				H				H
	21								
	22								H
	23				H				H
PT 7	24				H				H
	25								
	26								H
	27				H				H
PT 8	28				H			H	
	29							H	
	30			H				H	
	31				H		H	H	

H ≡ High ≡ Logic One ≡ Programmed

Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

Marked "K1"

Signetics 82S123

B15 on SDF

D30, B20 on DRU

# PROM Pattern for D9 and D10 on MIU Cards. H PROM 1-1024-5B

HDF. D10					
T.U.	1248.1248				
	0.0000	16.0006	32.0012	48.0019	
	0000.0000	0000.0110	1000.0100	1000.1001	
	1.0000	17.0007	33.0013	49.0019	
	0000.0000	0000.1110	1000.1100	1000.1001	
	2.0001	18.0007	34.0013	50.0020	
	0000.1000	0000.1110	1000.1100	0100.0000	
	3.0001	19.0007	35.0014	51.0020	
	0000.1000	0000.1110	1000.0010	0100.0000	
	4.0002	20.0008	36.0014	52.0020	
	0000.0100	0000.0001	1000.0010	0100.0000	
	5.0002	21.0008	37.0014	53.0021	
	0000.0100	0000.0001	1000.0010	0100.1000	
	6.0002	22.0009	38.0015	54.0021	
	0000.0100	0000.1001	1000.1010	0100.1000	
	7.0003	23.0009	39.0015	55.0021	
	0000.1100	0000.1001	1000.1010	0100.1000	
	8.0003	24.0009	40.0016	56.0022	
	0000.1100	0000.1001	1000.0110	0100.0100	
	9.0004	25.0010	41.0016	57.0022	
	0000.0010	1000.0000	1000.0110	0100.0100	
	10.0004	26.0010	42.0016	58.0023	
	0000.0010	1000.0000	1000.0110	0100.1100	
	11.0004	27.0011	43.0017	59.0023	
	0000.0010	1000.1000	1000.1110	0100.1100	
	12.0005	28.0011	44.0017	60.0023	
	0000.1010	1000.1000	1000.1110	0100.1100	
	13.0005	29.0011	45.0018	61.0024	
	0000.1010	1000.1000	1000.0001	0100.0010	
	14.0005	30.0012	46.0018	62.0024	
	0000.1010	1000.0100	1000.0001	0100.0010	
	15.0006	31.0012	47.0018	63.0025	
	0000.0110	1000.0100	1000.0001	0100.1010	

Decimal  
Output

Decimal  
PROM  
Address

O<sub>3</sub>O<sub>2</sub>O<sub>1</sub>O<sub>0</sub>

Outputs of  
D10 PROM

O=Low=Program

O<sub>3</sub>O<sub>2</sub>O<sub>1</sub>O<sub>0</sub>

Outputs of  
D9 PROM

O=Low=Program

64.0025	80.0031	96.0037	112.0044
0100.1010	1100.1000	1100.1110	0010.0010
65.0025	81.0032	97.0038	113.0044
0100.1010	1100.0100	1100.0001	0010.0010
66.0026	82.0032	98.0038	114.0045
0100.0110	1100.0100	1100.0001	0010.1010
67.0026	83.0032	99.0039	115.0045
0100.0110	1100.0100	1100.1001	0010.1010
68.0027	84.0033	100.0039	116.0045
0100.1110	1100.1100	1100.1001	0010.1010
69.0027	85.0033	101.0039	117.0046
0100.1110	1100.1100	1100.1001	0010.0110
70.0027	86.0034	102.0040	118.0046
0100.1110	1100.0010	0010.0000	0010.0110
71.0028	87.0034	103.0040	119.0046
0100.0001	1100.0010	0010.0000	0010.0110
72.0028	88.0034	104.0041	120.0047
0100.0001	1100.0010	0010.1000	0010.1110
73.0029	89.0035	105.0041	121.0047
0100.1001	1100.1010	0010.1000	0010.1110
74.0029	90.0035	106.0041	122.0048
0100.1001	1100.1010	0010.1000	0010.0001
75.0029	91.0036	107.0042	123.0048
0100.1001	1100.0110	0010.0100	0010.0001
76.0030	92.0036	108.0042	124.0048
1100.0000	1100.0110	0010.0100	0010.0001
77.0030	93.0036	109.0043	125.0049
1100.0000	1100.0110	0010.1100	0010.1001
78.0030	94.0037	110.0043	126.0049
1100.0000	1100.1110	0010.1100	0010.1001
79.0031	95.0037	111.0043	127.0050
1100.1000	1100.1110	0010.1100	1010.0000

128.0050	144.0056	160.0062	176.0069
1010.0000	1010.0110	0110.0100	0110.1001
129.0050	145.0057	161.0063	177.0069
1010.0000	1010.1110	0110.1100	0110.1001
130.0051	146.0057	162.0063	178.0070
1010.1000	1010.1110	0110.1100	1110.0000
131.0051	147.0057	163.0064	179.0070
1010.1000	1010.1110	0110.0010	1110.0000
132.0052	148.0058	164.0064	180.0070
1010.0100	1010.0001	0110.0010	1110.0000
133.0052	149.0058	165.0064	181.0071
1010.0100	1010.0001	0110.0010	1110.1000
134.0052	150.0059	166.0065	182.0071
1010.0100	1010.1001	0110.1010	1110.1000
135.0053	151.0059	167.0065	183.0071
1010.1100	1010.1001	0110.1010	1110.1000
136.0053	152.0059	168.0066	184.0072
1010.1100	1010.1001	0110.0110	1110.0100
137.0054	153.0060	169.0066	185.0072
1010.0010	0110.0000	0110.0110	1110.0100
138.0054	154.0060	170.0066	186.0073
1010.0010	0110.0000	0110.0110	1110.1100
139.0054	155.0061	171.0067	187.0073
1010.0010	0110.1000	0110.1110	1110.1100
140.0055	156.0061	172.0067	188.0073
1010.1010	0110.1000	0110.1110	1110.1100
141.0055	157.0061	173.0068	189.0074
1010.1010	0110.1000	0110.0001	1110.0010
142.0055	158.0062	174.0068	190.0074
1010.1010	0110.0100	0110.0001	1110.0010
143.0056	159.0062	175.0068	191.0075
1010.0110	0110.0100	0110.0001	1110.1010

192.0075	208.0081	224.0087	240.0094
1110.1010	0001.1000	0001.1110	1001.0010
193.0075	209.0082	225.0088	241.0094
1110.1010	0001.0100	0001.0001	1001.0010
194.0076	210.0082	226.0088	242.0095
1110.0110	0001.0100	0001.0001	1001.1010
195.0076	211.0082	227.0089	243.0095
1110.0110	0001.0100	0001.1001	1001.1010
196.0077	212.0083	228.0089	244.0095
1110.1110	0001.1100	0001.1001	1001.1010
197.0077	213.0083	229.0089	245.0096
1110.1110	0001.1100	0001.1001	1001.0110
198.0077	214.0084	230.0090	246.0096
1110.1110	0001.0010	1001.0000	1001.0110
199.0078	215.0084	231.0090	247.0096
1110.0001	0001.0010	1001.0000	1001.0110
200.0078	216.0084	232.0091	248.0097
1110.0001	0001.0010	1001.1000	1001.1110
201.0079	217.0085	233.0091	249.0097
1110.1001	0001.1010	1001.1000	1001.1110
202.0079	218.0085	234.0091	250.0098
1110.1001	0001.1010	1001.1000	1001.0001
203.0079	219.0086	235.0092	251.0098
1110.1001	0001.0110	1001.0100	1001.0001
204.0080	220.0086	236.0092	252.0098
0001.0000	0001.0110	1001.0100	1001.0001
205.0080	221.0086	237.0093	253.0099
0001.0000	0001.0110	1001.1100	1001.1001
206.0080	222.0087	238.0093	254.0099
0001.0000	0001.1110	1001.1100	1001.1001
207.0081	223.0087	239.0093	255.0100
0001.1000	0001.1110	1001.1100	0101.0000

# Coordinate Converter Altitude Error Correction (Card 2)

<u>Input Address</u>	F30				F26 LSB			
	D	C	B	A	Q	R	S	T
0-27	0	0	0	0	0	0	0	0
28-38	0	0	0	0	0	0	0	1
39-47	0	0	0	0	0	0	1	0
48-55	0	0	0	0	0	0	1	1
56-62	0	0	0	0	0	1	0	0
63-68	0	0	0	0	0	1	0	1
68-74	0	0	0	0	0	1	1	0
75-79	0	0	0	0	0	1	1	1
80	0	0	0	0	1	0	0	0
81	0	0	0	0	1	0	0	0
82	0	0	0	0	1	0	0	0
83	0	0	0	0	1	0	0	0
84	0	0	0	0	1	0	0	1
85	0	0	0	0	1	0	0	1
86	0	0	0	0	1	0	0	1
87	0	0	0	0	1	0	0	1
88	0	0	0	0	1	0	0	1
89	0	0	0	0	1	0	1	0
90	0	0	0	0	1	0	1	0
91	0	0	0	0	1	0	1	0
92	0	0	0	0	1	0	1	0
93	0	0	0	0	1	0	1	1
94	0	0	0	0	1	0	1	1
95	0	0	0	0	1	0	1	1
96	0	0	0	0	1	0	1	1
97	0	0	0	0	1	0	1	1
98	0	0	0	0	1	1	0	0
99	0	0	0	0	1	1	0	0
100	0	0	0	0	1	1	0	0
101	0	0	0	0	1	1	0	1
102	0	0	0	0	1	1	0	1

Coordinate Converter Altitude Error Correction (Card 2 ) (Cont)

<u>Input Address</u>	F30				F26 LSB			
	<u>D</u>	<u>C</u>	<u>B</u>	<u>A</u>	<u>Q</u>	<u>R</u>	<u>S</u>	<u>T</u>
103	0	0	0	0	1	1	0	1
104	0	0	0	0	1	1	0	1
105	0	0	0	0	1	1	1	0
106	0	0	0	0	1	1	1	0
107	0	0	0	0	1	1	1	0
108	0	0	0	0	1	1	1	1
109	0	0	0	0	1	1	1	1
110	0	0	0	0	1	1	1	1
111	0	0	0	0	1	1	1	1
112	0	0	0	1	0	0	0	0
113	0	0	0	1	0	0	0	0
114	0	0	0	1	0	0	0	0
115	0	0	0	1	0	0	0	0
116	0	0	0	1	0	0	0	1
117	0	0	0	1	0	0	0	1
118	0	0	0	1	0	0	0	1
119	0	0	0	1	0	0	1	0
120	0	0	0	1	0	0	1	0
121	0	0	0	1	0	0	1	0
122	0	0	0	1	0	0	1	1
123	0	0	0	1	0	0	1	1
124	0	0	0	1	0	0	1	1
125	0	0	0	1	0	1	0	0
126	0	0	0	1	0	1	0	0
127	0	0	0	1	0	1	0	0
128	0	0	0	1	0	1	0	1
129	0	0	0	1	0	1	0	1
130	0	0	0	1	0	1	0	1
131	0	0	0	1	0	1	0	1
132	0	0	0	1	0	1	1	0
133	0	0	0	1	0	1	1	0

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

<u>Input Address</u>	F30				F26 LSB			
	<u>D</u>	<u>C</u>	<u>B</u>	<u>A</u>	<u>Q</u>	<u>R</u>	<u>S</u>	<u>T</u>
134	0	0	0	1	0	1	1	0
135	0	0	0	1	0	1	1	1
136	0	0	0	1	0	1	1	1
137	0	0	0	1	1	0	0	0
138	0	0	0	1	1	0	0	0
139	0	0	0	1	1	0	0	0
140	0	0	0	1	1	0	0	1
141	0	0	0	1	1	0	0	1
142	0	0	0	1	1	0	1	0
143	0	0	0	1	1	0	1	0
144	0	0	0	1	1	0	1	0
145	0	0	0	1	1	0	1	1
146	0	0	0	1	1	0	1	1
147	0	0	0	1	1	0	1	1
148	0	0	0	1	1	1	0	0
149	0	0	0	1	1	1	0	0
150	0	0	0	1	1	1	0	1
151	0	0	0	1	1	1	0	1
152	0	0	0	1	1	1	0	1
153	0	0	0	1	1	1	1	0
154	0	0	0	1	1	1	1	0
155	0	0	0	1	1	1	1	0
156	0	0	0	1	1	1	1	1
157	0	0	0	1	0	0	0	0
158	0	0	1	0	0	0	0	0
159	0	0	1	0	0	0	0	0
160	0	0	1	0	0	0	0	0
161	0	0	1	0	0	0	0	1
162	0	0	1	0	0	0	0	1
163	0	0	1	0	0	0	1	0

# Coordinate Converter Altitude Error Correction (Card 2) (Cont)

<u>Input Address</u>	F30				F26 LSB			
	<u>D</u>	<u>C</u>	<u>B</u>	<u>A</u>	<u>Q</u>	<u>R</u>	<u>S</u>	<u>T</u>
164	0	0	1	0	0	0	1	0
165	0	0	1	0	0	0	1	0
166	0	0	1	0	0	0	1	1
167	0	0	1	0	0	0	1	1
168	0	0	1	0	0	1	0	0
169	0	0	1	0	0	1	0	0
170	0	0	1	0	0	1	0	1
171	0	0	1	0	0	1	0	1
172	0	0	1	0	0	1	0	1
173	0	0	1	0	0	1	1	0
174	0	0	1	0	0	1	1	0
175	0	0	1	0	0	1	1	1
176	0	0	1	0	0	1	1	1
177	0	0	1	0	1	0	0	0
178	0	0	1	0	1	0	0	0
179	0	0	1	0	1	0	0	1
180	0	0	1	0	1	0	0	1
181	0	0	1	0	1	0	1	0
182	0	0	1	0	1	0	1	0
183	0	0	1	0	1	0	1	0
184	0	0	1	0	1	0	1	1
185	0	0	1	0	1	0	1	1
186	0	0	1	0	1	1	0	0
187	0	0	1	0	1	1	0	0
188	0	0	1	0	1	1	0	1
189	0	0	1	0	1	1	0	1
190	0	0	1	0	1	1	1	0
191	0	0	1	0	1	1	1	0
192	0	0	1	0	1	1	1	1
193	0	0	1	0	1	1	1	1
194	0	0	1	1	0	0	0	0

# Coordinate Converter Altitude Error Correction (Card 2) (Cont)

<u>Input Address</u>	F30				F26 LSB			
	<u>D</u>	<u>C</u>	<u>B</u>	<u>A</u>	<u>Q</u>	<u>R</u>	<u>S</u>	<u>T</u>
195	0	0	1	1	0	0	0	0
196	0	0	1	1	0	0	0	1
197	0	0	1	1	0	0	0	1
198	0	0	1	1	0	0	1	0
199	0	0	1	1	0	0	1	0
200	0	0	1	1	0	0	1	1
201	0	0	1	1	0	0	1	1
202	0	0	1	1	0	1	0	0
203	0	0	1	1	0	1	0	0
204	0	0	1	1	0	1	0	1
205	0	0	1	1	0	1	0	1
206	0	0	1	1	0	1	1	0
207	0	0	1	1	0	1	1	0
208	0	0	1	1	0	1	1	1
209	0	0	1	1	0	1	1	1
210	0	0	1	1	1	0	0	0
211	0	0	1	1	1	0	0	0
212	0	0	1	1	1	0	0	1
213	0	0	1	1	1	0	1	0
214	0	0	1	1	1	0	1	0
215	0	0	1	1	1	0	1	1
216	0	0	1	1	1	0	1	1
217	0	0	1	1	1	1	0	0
218	0	0	1	1	1	1	0	0
219	0	0	1	1	1	1	0	1
220	0	0	1	1	1	1	0	1
221	0	0	1	1	1	1	1	0
222	0	0	1	1	1	1	1	1
223	0	0	1	1	1	1	1	1

Coordinate Converter Altitude Error Correction (Card 2) (Cont)

<u>Input Address</u>	F30				F26 LSB			
	<u>D</u>	<u>C</u>	<u>B</u>	<u>A</u>	<u>Q</u>	<u>R</u>	<u>S</u>	<u>T</u>
224	0	1	0	0	0	0	0	0
225	0	1	0	0	0	0	0	1
226	0	1	0	0	0	0	0	1
227	0	1	0	0	0	0	1	0
228	0	1	0	0	0	0	1	0
229	0	1	0	0	0	0	1	1
230	0	1	0	0	0	0	1	1
231	0	1	0	0	0	1	0	0
232	0	1	0	0	0	1	0	0
233	0	1	0	0	0	1	0	1
234	0	1	0	0	0	1	0	1
235	0	1	0	0	0	1	1	0
236	0	1	0	0	0	1	1	0
237	0	1	0	0	0	1	1	1
238	0	1	0	0	1	0	0	0
239	0	1	0	0	1	0	0	1
240	0	1	0	0	1	0	0	1
241	0	1	0	0	1	0	1	0
242	0	1	0	0	1	0	1	0
243	0	1	0	0	1	0	1	1
244	0	1	0	0	1	1	0	0
245	0	1	0	0	1	1	0	0
246	0	1	0	0	1	1	0	1
247	0	1	0	0	1	1	1	0
248	0	1	0	0	1	1	1	0
249	0	1	0	0	1	1	1	1
250	0	1	0	1	0	0	0	0
251	0	1	0	1	0	0	0	0

# Coordinate Converter Altitude Error Correction (Card 2) (Cont)

<u>Input Address</u>	F30				F26				LSB
	<u>D</u>	<u>C</u>	<u>B</u>	<u>A</u>	<u>Q</u>	<u>R</u>	<u>S</u>	<u>T</u>	
252	0	1	0	1	0	0	0	1	
253	0	1	0	1	0	0	1	0	
254	0	1	0	1	0	0	1	0	
255	0	1	0	1	0	0	1	1	

# DCU Card, Character Generator ROM

5 X 7 CHARACTER FONT\*

MM6055

A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

ASCII INPUT ADDRESS	B <sub>1</sub> B <sub>2</sub> B <sub>3</sub> A <sub>3</sub> A <sub>4</sub> A <sub>5</sub> 000	A <sub>3</sub> A <sub>4</sub> A <sub>5</sub> 100	A <sub>3</sub> A <sub>4</sub> A <sub>5</sub> 010	A <sub>3</sub> A <sub>4</sub> A <sub>5</sub> 110	A <sub>3</sub> A <sub>4</sub> A <sub>5</sub> 001	A <sub>3</sub> A <sub>4</sub> A <sub>5</sub> 101	A <sub>3</sub> A <sub>4</sub> A <sub>5</sub> 011	A <sub>3</sub> A <sub>4</sub> A <sub>5</sub> 111
B <sub>4</sub> B <sub>5</sub> B <sub>6</sub> A <sub>6</sub> A <sub>7</sub> A <sub>8</sub> 000								
A <sub>6</sub> A <sub>7</sub> A <sub>8</sub> 100								
A <sub>6</sub> A <sub>7</sub> A <sub>8</sub> 010								
A <sub>6</sub> A <sub>7</sub> A <sub>8</sub> 110								
A <sub>6</sub> A <sub>7</sub> A <sub>8</sub> 001								
A <sub>6</sub> A <sub>7</sub> A <sub>8</sub> 101								
A <sub>6</sub> A <sub>7</sub> A <sub>8</sub> 011								
A <sub>6</sub> A <sub>7</sub> A <sub>8</sub> 111								

\*FROM THE USASCII CODE A<sub>8</sub> B<sub>7</sub> B<sub>6</sub>

## DDI Card, B23 Signetics 82S123 (32 x 8)

Address					Unconditional Next State				
	MEISB B7	MEISA B6	SATNE B5	CNSS B4	UNSD B3	UNSC B2	UNSB B1	UNSA B0	
0		H		H					0
1		H	H	H				H	1
2	H						H		2
3	H					H		H	3
4	H			H			H		4
5	H	H					H	H	5
6	H						H	H	6
7			H		H			H	7
8	H	H					H	H	8
9	H	H			H	H	H		9
10	H	H			H				10
11		H			H		H	H	11
12									12
13									13
14									14
15	H	H			H	H			15
16		H							16
17		H					H	H	17
18		H					H		18
19		H				H		H	19
20		H		H			H		20
21	H	H					H	H	21
22		H					H	H	22
23									23
24									24
25									25
26									26
27									27
28									28
29									29
30									30
31									31

H = High = Logic One = Programmed  
 Blank = Low = Logic Zero = Not Programmed

## DDI Card, B29 Signetics 82S123 (32 x 8)

Address					Conditional Next State				
	B7	B6	B5	MWGI B4	CNSD B3	CNSC B2	CNSB B1	CNSA B0	
0							H	H	0
1							H	H	1
2							H	H	2
3									3
4							H	H	4
5							H	H	5
6									6
7									7
8							H	H	8
9							H	H	9
10							H	H	10
11							H	H	11
12									12
13							H	H	13
14					H		H		14
15									15
16				H			H		16
17				H			H	H	17
18				H		H	H	H	18
19									19
20						H			20
21						H	H		21
22									22
23									23
24									24
25									25
26									26
27									27
28									28
29									29
30									30
31									31

H ≡ High ≡ Logic One ≡ Programmed

Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

# SIGNETICS 82S123 C28 ON MAG CARD

	<u>TS4</u>	4	3	2	1	<u>TS3</u>	<u>TS2</u>	<u>TS1</u>	
Address	B7	B6	B5	B4	B3	B2	B1	B0	
0			H	H		H	H		0
1				H	H		H	H	1
2	H	H			H			H	2
3	H	H	H			H			3
4	H		H	H		H	H	H	4
5	H			H	H	H	H	H	5
6	H	H			H	H	H	H	6
7	H	H	H			H	H	H	7
8			H	H	H	H	H	H	8
9	H	H		H	H		H	H	9
10	H	H	H		H	H		H	10
11	H	H	H	H		H	H		11
12	H		H	H	H	H	H	H	12
13	H	H		H	H	H	H	H	13
14	H	H	H		H	H	H	H	14
15	H	H	H	H		H	H	H	15
16									16
17									17
18									18
19									19
20									20
21									21
22									22
23									23
24									24
25									25
26									26
27									27
28									28
29									29
30									30
31									31

H ■ High ■ Logic One ■ Programmed  
Blank ■ Low ■ Logic Zero ■ Not Programmed

# MAG CODE CONV. PROMS (SIGNETICS 82S129)

ADR	MAG D9 8421	MAG D8 8421	ADR	MAG D9 8421	MAG D8 8421	ADR	MAG D9 8421	MAG D8 8421	ADR	MAG D9 8421	MAG D8 8421
000	....	....	040	.H..	....	080	H...	....	120	HH..	....
001	....	...H	041	.H..	...H	081	H...	...H	121	HH..	...H
002	....	..H.	042	.H..	..H.	082	H...	..H.	122	HH..	..H.
003	....	..HH	043	.H..	..HH	083	H...	..HH	123	HH..	..HH
004	....	.H..	044	.H..	.H..	084	H...	.H..	124	HH..	.H..
005	....	H...	045	.H..	H...	085	H...	H...	125	HH..	H...
006	....	H..H	046	.H..	H..H	086	H...	H..H	126	HH..	H..H
007	....	H.H.	047	.H..	H.H.	087	H...	H.H.	127	HH..	H.H.
008	....	H.HH	048	.H..	H.HH	088	H...	H.HH	128	HH..	H.HH
009	....	HH..	049	.H..	HH..	089	H...	HH..	129	HH..	HH..
010	...H	....	050	.H.H	....	090	H..H	....	130	HH.H	....
011	...H	...H	051	.H.H	...H	091	H..H	...H	131	HH.H	...H
012	...H	..H.	052	.H.H	..H.	092	H..H	..H.	132	HH.H	..H.
013	...H	..HH	053	.H.H	..HH	093	H..H	..HH	133	HH.H	..HH
014	...H	.H..	054	.H.H	.H..	094	H..H	.H..	134	HH.H	.H..
015	...H	H...	055	.H.H	H...	095	H..H	H...	135	HH.H	H...
016	...H	H..H	056	.H.H	H..H	096	H..H	H..H	136	HH.H	H..H
017	...H	H.H.	057	.H.H	H.H.	097	H..H	H.H.	137	HH.H	H.H.
018	...H	H.HH	058	.H.H	H.HH	098	H..H	H.HH	138	HH.H	H.HH
019	...H	HH..	059	.H.H	HH..	099	H..H	HH..	139	HH.H	HH..
020	..H.	....	060	.HH.	....	100	H.H.	....	140	HHH.	....
021	..H.	...H	061	.HH.	...H	101	H.H.	...H	141	HHH.	...H
022	..H.	..H.	062	.HH.	..H.	102	H.H.	..H.	142	HHH.	..H.
023	..H.	..HH	063	.HH.	..HH	103	H.H.	..HH	143	HHH.	..HH
024	..H.	.H..	064	.HH.	.H..	104	H.H.	.H..	144	HHH.	.H..
025	..H.	H...	065	.HH.	H...	105	H.H.	H...	145	HHH.	H...
026	..H.	H..H	066	.HH.	H..H	106	H.H.	H..H	146	HHH.	H..H
027	..H.	H.H.	067	.HH.	H.H.	107	H.H.	H.H.	147	HHH.	H.H.
028	..H.	H.HH	068	.HH.	H.HH	108	H.H.	H.HH	148	HHH.	H.HH
029	..H.	HH..	069	.HH.	HH..	109	H.H.	HH..	149	HHH.	HH..
030	..HH	....	070	.HHH	....	110	H.HH	....	150	HHHH	....
031	..HH	...H	071	.HHH	...H	111	H.HH	...H	151	HHHH	...H
032	..HH	..H.	072	.HHH	..H.	112	H.HH	..H.	152	HHHH	..H.
033	..HH	..HH	073	.HHH	..HH	113	H.HH	..HH	153	HHHH	..HH
034	..HH	.H..	074	.HHH	.H..	114	H.HH	.H..	154	HHHH	.H..
035	..HH	H...	075	.HHH	H...	115	H.HH	H...	155	HHHH	H...
036	..HH	H..H	076	.HHH	H..H	116	H.HH	H..H	156	HHHH	H..H
037	..HH	H.H.	077	.HHH	H.H.	117	H.HH	H.H.	157	HHHH	H.H.
038	..HH	H.HH	078	.HHH	H.HH	118	H.HH	H.HH	158	HHHH	H.HH
039	..HH	HH..	079	.HHH	HH..	119	H.HH	HH..	159	HHHH	HH..

H = High = Logic 1 = Programmed

# MAG ROTATION PROMS (SIGNETICS 82S131)

ADR	MAG C13 8421	MAG C11 8421	ADR	MAG C13 8421	MAG C11 8421	ADR	MAG C13 8421	MAG C11 8421	ADR	MAG C13 8421	MAG C11 8421
000	....	....	064	....	..H.	128	....	..H.	192	....	..HH.
001	....	....H	065	....	..HH	129	....	..H.H	193	....	..HHH
002	....	....H	066	....	..H.	130	....	..HH.	194	....	..H...
003	....	....HH	067	....	..H.H	131	....	..HHH	195	....	..H..H
004	....	....H.	068	....	..HH.	132	....	..H...	196	....	..H..H
005	....	....H.H	069	....	..HHH	133	....	..H..H	197	....	..H.HH
006	....	....HH.	070	....	..H...	134	....	..H..H	198	....	..HH.
007	....	....HHH	071	....	..H..H	135	....	..H.HH	199	....	..HH..H
008	....	....H...	072	....	..H..H.	136	....	..HH.	200	....	..HHH.
009	....	....H..H	073	....	..H.HH	137	....	..HH.H	201	....	..HHHH
010	....	....H..H.	074	....	..H.H...	138	....	..HHH.	202	....	..H....
011	....	....H.HH	075	....	..H.H.H	139	....	..HHHH	203	....	..H....H
012	....	....HH.	076	....	..HHH.	140	....	..H....	204	....	..H....H
013	....	....HH..H	077	....	..HHHH	141	....	..H....H	205	....	..H....H
014	....	....HHH.	078	....	..H....	142	....	..H....H	206	....	..H....H
015	....	....HHHH	079	....	..H....H	143	....	..H....H	207	....	..H....H
016	....	....H....	080	....	..H....H	144	....	..H....H	208	....	..HH..H
017	....	....H....H	081	....	..H....H	145	....	..H....H	209	....	..HHH.
018	....	....H....H.	082	....	..H....H.	146	....	..HH.	210	....	..H....
019	....	....H....HH	083	....	..H....H.H	147	....	..HHH.	211	....	....
020	....	....H....H.	084	....	..H....H.	148	....	..H....H	212	....	....H....
021	....	....H....H.H	085	....	..H....HHH	149	....	....	213	....	....H....
022	....	....H....HH.	086	....	..H....H...	150	....	....H....	214	....	....HH.
023	....	....H....HHH	087	....	....	151	....	....H....	215	....	....H....
024	....	....H....H....	088	....	....H....	152	....	....HH.	216	....	....H....H
025	....	....H....H..H	089	....	....H....H.	153	....	....H....H	217	....	....H....H
026	....	....H....H..H.	090	....	....H....H.H	154	....	....H....H	218	....	....H....H
027	....	....H....H.HH	091	....	....H....HH	155	....	....H....HH	219	....	....H....HH
028	....	....H....HH..	092	....	....H....HH.	156	....	....H....HH.	220	....	....H....
029	....	....H....HH..H	093	....	....H....HH..H	157	....	....H....HH.H	221	....	....H....H
030	....	....H....HHH.	094	....	....H....HHH.	158	....	....H....HHH.	222	....	....H....HHH.
031	....	....H....HHHH	095	....	....H....HHHH	159	....	....H....HHHH	223	....	....H....HHHH
032	....	....H....	096	....	....H....HH	160	....	....H....H.	224	....	....HHH.
033	....	....H....	097	....	....H....H.	161	....	....H....H.	225	....	....H....
034	....	....H....HH	098	....	....H....H.H	162	....	....H....HHH	226	....	....H....H
035	....	....H....H.	099	....	....H....HH.	163	....	....H....H.	227	....	....H....H.
036	....	....H....H..H	100	....	....H....HHH	164	....	....H....H.H	228	....	....H....HH
037	....	....H....HH.	101	....	....H....H....	165	....	....H....H.H	229	....	....H....HH.
038	....	....H....HHH	102	....	....H....H..H	166	....	....H....HH	230	....	....H....HH
039	....	....H....H....	103	....	....H....H..H.	167	....	....H....HH.	231	....	....H....HHH.
040	....	....H....H....H	104	....	....H....H..HH	168	....	....H....HH.H	232	....	....H....HHH.
041	....	....H....H..H.	105	....	....H....HH.	169	....	....H....HHH.	233	....	....H....
042	....	....H....H.HH	106	....	....H....HH..H	170	....	....H....HHHH	234	....	....H....H
043	....	....H....HH.	107	....	....H....HHH.	171	....	....H....	235	....	....H....H.
044	....	....H....HH..H	108	....	....H....HHHH	172	....	....H....H.	236	....	....H....HH
045	....	....H....HHH.	109	....	....H....	173	....	....H....H.	237	....	....H....H.
046	....	....H....HHHH	110	....	....H....H.	174	....	....H....HH	238	....	....H....H.H
047	....	....H....	111	....	....H....H..H.	175	....	....H....H.	239	....	....H....HH.
048	....	....H....H....	112	....	....H....H..HH	176	....	....H....H.H	240	....	....H....HHH.
049	....	....H....H..H.	113	....	....H....H..H.	177	....	....H....HH.	241	....	....H....
050	....	....H....HH	114	....	....H....H..H.H	178	....	....H....HHH	242	....	....
051	....	....H....H....	115	....	....H....HH.	179	....	....H....H.	243	....	....H....H
052	....	....H....H..H	116	....	....H....HHH	180	....	....	244	....	....H....H.
053	....	....H....HH.	117	....	....H....H....	181	....	....H....H.	245	....	....H....HH
054	....	....H....HHH	118	....	....	182	....	....H....H.	246	....	....H....H.
055	....	....H....H....	119	....	....H....H....	183	....	....H....HH	247	....	....H....H.H
056	....	....H....H....	120	....	....H....H....	184	....	....H....H.	248	....	....H....HH.
057	....	....H....H..H	121	....	....H....H..H	185	....	....H....H.H	249	....	....H....H.H
058	....	....H....H..H.	122	....	....H....H..H.	186	....	....H....H.H	250	....	....H....H.H
059	....	....H....H..HH	123	....	....H....H..HH	187	....	....H....HH	251	....	....H....HH
060	....	....H....HH..	124	....	....H....HH..	188	....	....H....HH.	252	....	....H....HH.
061	....	....H....HH..H	125	....	....H....HH..H	189	....	....H....HH.H	253	....	....H....HH.H
062	....	....H....HHH.	126	....	....H....HHH.	190	....	....H....HHH.	254	....	....H....HHH.
063	....	....H....HHHH	127	....	....H....HHHH	191	....	....H....HHHH	255	....	....H....HHHH

H = High = Logic 1 = Programmed

# MAG ROTATION PROMS (Continued)

ADR	MAG C13 8421	MAG C11 8421	ADR	MAG C13 8421	MAG C11 8421	ADR	MAG C13 8421	MAG C11 8421	ADR	MAG C13 8421	MAG C11 8421
256	....	H...	320	....	H..H.	384	....	HH..	448	....	HHH.
257	....	H..H	321	....	H..HH	385	....	HH..H	449	....	HHHH
258	....	H..H.	322	....	HH..	386	....	HHH.	450	....	H...
259	....	H..HH	323	....	HH..H	387	....	HHHH	451	....	H..H
260	....	HH..	324	....	HHH.	388	....	H...	452	....	H..H
261	....	HH..H	325	....	HHHH	389	....	H..H	453	....	H..H
262	....	HHH.	326	....	H...	390	....	H..H	454	....	H..H
263	....	HHHH	327	....	H..H	391	....	H..HH	455	....	H..H
264	....	H...	328	....	H..H.	392	....	H..H.	456	....	H..H
265	....	H..H	329	....	H..HH	393	....	H..H	457	....	H..HH
266	....	H..H.	330	....	H..H.	394	....	H..H.	458	....	H...
267	....	H..HH	331	....	H..H	395	....	H..HH	459	....	H...
268	....	H..H.	332	....	H..HH	396	....	H..H.	460	....	H..H
269	....	H..H	333	....	H..HH	397	....	H...	461	....	H..H
270	....	H..HH.	334	....	H..H.	398	....	H..H.	462	....	H..HH
271	....	H..HHH	335	....	H...	399	....	H..H.	463	....	H..H.
272	....	H..H.	336	....	H..H.	400	....	H..HH	464	....	H..H
273	....	H...	337	....	H..H.	401	....	H..H.	465	....	H..HH
274	....	H..H	338	....	H..HH	402	....	H..H.	466	....	H..HH
275	....	H..H.	339	....	H..H.	403	....	H..HH	467	....	H..H.
276	....	H..HH	340	....	H..H	404	....	H..HH	468	....	H..H
277	....	H..H.	341	....	H..HH	405	....	H..H.	469	....	H..H.
278	....	H..H	342	....	H..HH	406	....	H..H	470	....	H..HH
279	....	H..HH.	343	....	H..H.	407	....	H..H.	471	....	H..H.
280	....	H..HHH	344	....	H..H	408	....	H..HH	472	....	H..H
281	....	H..H	345	....	H..H	409	....	H..H	473	....	H..H
282	....	H..H.	346	....	H..H.	410	....	H..H.	474	....	H..H
283	....	H..HH	347	....	H..HH	411	....	H..HH	475	....	H..HH
284	....	H..H.	348	....	H..HH.	412	....	H..HH.	476	....	H..H.
285	....	H..HH	349	....	H..HH	413	....	H..HH	477	....	H..HH
286	....	H..HHH	350	....	H..HHH	414	....	H..HHH	478	....	H..HHH
287	....	H..HHHH	351	....	H..HHHH	415	....	H..HHHH	479	....	H..HHHH
288	....	H..H.	352	....	H..HH	416	....	H..HH	480	....	H..HHH
289	....	H..H.	353	....	H..HH.	417	....	H..HH.	481	....	H..H.
290	....	H..HH	354	....	H..HH	418	....	H..HHH	482	....	H..H
291	....	H..H.	355	....	H..HH.	419	....	H..H.	483	....	H..H.
292	....	H..HH	356	....	H..HHH	420	....	H..H.	484	....	H..HH
293	....	H..HHH	357	....	H..H.	421	....	H..H.	485	....	H..H.
294	....	H..HHHH	358	....	H..H.	422	....	H..HH	486	....	H..H
295	....	H..H.	359	....	H..H.	423	....	H..H.	487	....	H..H.
296	....	H..H.	360	....	H..HH	424	....	H..H	488	....	H..HH
297	....	H..H.	361	....	H..H.	425	....	H..HH	489	....	H..H.
298	....	H..HH	362	....	H..H	426	....	H..HH	490	....	H..H.
299	....	H..H.	363	....	H..HH.	427	....	H..H.	491	....	H..H
300	....	H..H	364	....	H..HHH	428	....	H..H.	492	....	H..H.
301	....	H..HH	365	....	H..H.	429	....	H..H.	493	....	H..HH
302	....	H..HHH	366	....	H..H.	430	....	H..H.	494	....	H..H.
303	....	H..H.	367	....	H..H.	431	....	H..HH	495	....	H..H
304	....	H..H.	368	....	H..H.	432	....	H..H.	496	....	H..H.
305	....	H..H.	369	....	H..HH	433	....	H..H	497	....	H..HH
306	....	H..H.	370	....	H..H.	434	....	H..HH	498	....	H..H.
307	....	H..HH	371	....	H..H	435	....	H..HH	499	....	H..H
308	....	H..H.	372	....	H..HH.	436	....	H..H.	500	....	H..H.
309	....	H..H	373	....	H..HHH	437	....	H..H	501	....	H..HH
310	....	H..HH.	374	....	H..H.	438	....	H..H.	502	....	H..H.
311	....	H..HHH	375	....	H..H	439	....	H..HH	503	....	H..HH
312	....	H..H.	376	....	H..H.	440	....	H..HH.	504	....	H..HH.
313	....	H..H	377	....	H..HH	441	....	H..H.	505	....	H..H
314	....	H..H.	378	....	H..H.	442	....	H..H.	506	....	H..H.
315	....	H..HH	379	....	H..HH	443	....	H..HH	507	....	H..HH
316	....	H..H.	380	....	H..HH.	444	....	H..HH.	508	....	H..H.
317	....	H..HH	381	....	H..HH	445	....	H..HH	509	....	H..H
318	....	H..HHH	382	....	H..HHH	446	....	H..HH.	510	....	H..HH.
319	....	H..HHHH	383	....	H..HHH	447	....	H..HHH	511	....	H..HHH

# MAG ROTATION PROMS (Continued)

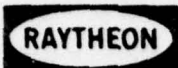
ADR	MAG C14 8421	MAG C12 8421	ADR	MAG C14 8421	MAG C12 8421	ADR	MAG C14 8421	MAG C12 8421	ADR	MAG C14 8421	MAG C12 8421
000	...H	....	072	....	...H	144	....	H.HH	216	...H	.H.H
001	...H	...H	073	....	...H	145	....	HH..	217	...H	H..H
002	...H	...H	074	....	...HH	146	....	HH.H	218	...H	H.H.
003	...H	...HH	075	....	...H	147	....	HHH.	219	...H	H.HH
004	...H	...H	076	....	...H.H	148	....	HHHH	220	...H	HH..
005	...H	...H.H	077	....	...HH	149	...H	....	221	...H	HH.H
006	...H	...HH	078	....	...HHH	150	...H	...H	222	...H	HHH.
007	...H	...HHH	079	....	...H...	151	...H	...H	223	...H	HHHH
008	...H	...H...	080	....	...H..H	152	...H	...HH	224	...H	HHH.
009	....	....	081	....	...H.H	153	...H	...H	225	...H	H...
010	....	...H	082	....	...H.HH	154	...H	...H	226	....	....
011	....	...H	083	....	...HH	155	...H	...HH	227	....	...H
012	....	...HH	084	....	...HH.H	156	...H	...HH	228	....	...H
013	....	...H	085	....	...HHH	157	...H	...HH.H	229	....	...HH
014	....	...H.H	086	....	...HHHH	158	...H	...HHH	230	....	...H
015	....	...HH	087	...H	....	159	...H	...HHHH	231	....	...H.H
016	....	...HHH	088	...H	...H	160	...H	...H	232	....	...HH
017	....	...H...	089	...H	...H.H	161	...H	...HH	233	....	...HHH
018	....	...H.H	090	...H	...H.H	162	...H	...HHH	234	....	...H...
019	....	...H.H	091	...H	...H.HH	163	...H	...H...	235	....	...H.H
020	....	...H.HH	092	...H	...HH	164	....	....	236	....	...H.H
021	....	...HH	093	...H	...HH.H	165	....	...H	237	....	...HHH
022	....	...HH.H	094	...H	...HHH	166	....	...H	238	....	...HH
023	....	...HHH	095	...H	...HHHH	167	....	...HH	239	....	...HH.H
024	....	...HHHH	096	...H	...HH	168	....	...H	240	....	...HHH
025	...H	...H.H	097	...H	...H	169	....	...H.H	241	....	...HHHH
026	...H	...H.H	098	...H	...H.H	170	....	...HH	242	...H	....
027	...H	...H.HH	099	...H	...HH	171	....	...HHH	243	...H	...H
028	...H	...HH	100	...H	...HHH	172	....	...H...	244	...H	...H
029	...H	...HH.H	101	...H	...H...	173	....	...H.H	245	...H	...HH
030	...H	...HHH	102	....	....	174	....	...H.H	246	...H	...H
031	...H	...HHHH	103	....	...H	175	....	...HH	247	...H	...H
032	...H	...H	104	....	...H	176	....	...HH	248	...H	...HH
033	...H	...H	105	....	...HH	177	....	...HH.H	249	...H	...H
034	...H	...HH	106	....	...H	178	....	...HHH	250	...H	...H
035	...H	...H	107	....	...H.H	179	....	...HHHH	251	...H	...HH
036	...H	...H.H	108	....	...HH	180	...H	....	252	...H	...HH
037	...H	...HH	109	....	...HHH	181	...H	...H	253	...H	...HH
038	...H	...HHH	110	....	...H	182	...H	...H	254	...H	...HH
039	...H	...H...	111	....	...H.H	183	...H	...HH	255	...H	...HHH
040	....	....	112	....	...H.H	184	...H	...H	256	...H	...H
041	....	...H	113	....	...H.HH	185	...H	...H	257	....	....
042	....	...H	114	....	...HH	186	...H	...H	258	....	...H
043	....	...HH	115	....	...HH.H	187	...H	...HH	259	....	...H
044	....	...H	116	....	...HHH	188	...H	...HH	260	....	...HH
045	....	...H.H	117	....	...HHHH	189	...H	...HH.H	261	....	...H
046	....	...HH	118	...H	....	190	...H	...HHH	262	....	...H.H
047	....	...HHH	119	...H	...H	191	...H	...HHHH	263	....	...HH
048	....	...H...	120	...H	...H	192	...H	...HH	264	....	...HHH
049	....	...H.H	121	...H	...H.H	193	...H	...HHH	265	....	...H...
050	....	...H.H	122	...H	...H.H	194	...H	...H...	266	....	...H.H
051	....	...H.HH	123	...H	...H.HH	195	....	....	267	....	...H.H
052	....	...HH	124	...H	...HH	196	....	...H	268	....	...HH
053	....	...HH.H	125	...H	...HH.H	197	....	...H	269	....	...HH
054	....	...HHH	126	...H	...HHH	198	....	...HH	270	....	...HH.H
055	....	...HHHH	127	...H	...HHHH	199	....	...H	271	....	...HHH
056	...H	....	128	...H	...H	200	....	...H.H	272	....	...HHHH
057	...H	...H.H	129	...H	...H.H	201	....	...HH	273	...H	....
058	...H	...H.H	130	...H	...HH	202	....	...HHH	274	...H	...H
059	...H	...H.HH	131	...H	...HHH	203	....	...H	275	...H	...H
060	...H	...HH	132	...H	...H...	204	....	...H.H	276	...H	...HH
061	...H	...HH.H	133	....	....	205	....	...H.H	277	...H	...H
062	...H	...HHH	134	....	...H	206	....	...H.HH	278	...H	...H.H
063	...H	...HHHH	135	....	...H	207	....	...HH	279	...H	...HH
064	...H	...H	136	....	...HH	208	....	...HH.H	280	...H	...HHH
065	...H	...HH	137	....	...H	209	....	...HHH	281	...H	...H
066	...H	...H	138	....	...H.H	210	....	...HHHH	282	...H	...H
067	...H	...H.H	139	....	...HH	211	...H	....	283	...H	...HH
068	...H	...HH	140	....	...HHH	212	...H	...H	284	...H	...H
069	...H	...HHH	141	....	...H	213	...H	...H	285	...H	...HH
070	...H	...H...	142	....	...H.H	214	...H	...HH	286	...H	...HH
071	....	....	143	....	...H.H	215	...H	...H	287	...H	...HHH

APPENDIX C

MEMORANDA

"Display Data Port Programming" (A.J. Jagodnik, Jr. memo #AJJ-21)

"Scan Converter Drawing List" (A.J. Jagodnik, Jr. memo #AJJ-49)



FORM 10-0557 (9-65) BOND

DIVISION Equipment  
Operation ADL  
Department ADL

To J. H. Turner

From A. J. Jagodnik, Jr.

Subject Display Data Port Programming

Classification Unclassified  
Contract No. DNA001-75-C-0050  
Distribution As Listed  
File No. -  
Memo No. AJJ-21  
Date 26 March 1975

- Reference: 1. AJJ-17, "Design Plan for the Display Data Interface of the Liquid Water Content Analyzer System," dated 17 Dec. 1974  
2. Scan Converter and Contour Refresh Memory Equipment Information Report, June 1974.

The Display Data Interface design plan contains sections entitled "Operation of the LWCA Control Panel" and "Hardware/Software Interaction". The purpose of this memo is to expand upon the contents of these sections, based upon the existing hardware which differs slightly from that originally planned. The programmer should find here information needed to write assembly language programs for the purpose of communicating between the scan converter color displays and the analyzer (Interdata 7/32 minicomputer).

The first section consists of operating instructions for the LWCA control panel and scan conversion processor, while subsequent sections discuss addressing conventions and each of the three basic types of data transfers: Write Display Memory, Read Display Memory, and Cursor Data Entry. Programming examples are also included.

#### Operation of the LWCA Scan Converter

Scan converter operation is covered in Reference 2; the information presented here is intended to serve as a supplement and covers operation with the LWCA Control Panel illustrated in Figure 1. Except for the ERASE DISPLAY buttons, all of the switches on the control panel also serve as indicators controlled by their state and/or the DDI (Display Data Interface) within the scan converter. An exception is the control labeled DATA SOURCE TAPE which functions only as an indicator to denote the fact that the Precision Digital Video Integrator has been set to accept data from Mag Tape for display on the scan converter.

The LWCA TO DISPLAY controls, when lit, indicate that write and/or read data transfers are enabled in the hardware. They are affected by several controls on the Scan Conversion Processor as indicated in Table 1. The state of these controls can be uniquely determined from the status byte of the Display Data Port which has been assigned device number X'8B'.

Table 1

Scan Conv. Controls		LWCA to Display				Device X'8B' Status Byte							
		Switches		Indicators									
Mode	Memory Control Store Video	Write On/Off	Read On/Off	Write On/Off	Read On/Off	0	1	2	3	4	5	6	7
A	All OFF	X	X	Lit	Lit	x	x	x	1	x	1	1	1
A	One or More ON	X	X	Dark	Lit	x	x	x	1	x	0	1	0
Not A	All OFF	Off	Off	Dark	Dark	x	x	x	0	x	0	0	1
		Off	On	Dark	Lit	x	x	x	0	x	0	1	1
		On	Off	Lit	Dark	x	x	x	0	x	1	0	1
		On	On	Lit	Lit	x	x	x	0	x	1	1	1
Not A	One or More ON	X	Off	Dark	Dark	x	x	x	0	x	0	0	0
			On	Dark	Lit	x	x	x	0	x	0	1	0
				X = don't care									

X = don't care

The scan converter will operate normally in the following mode switch positions: PPI, RHI, CAPPI and B. If the appropriate LWCA TO DISPLAY indicator is lit, the analyzer can read or write into the display memories. In mode switch position A, the necessary conditions for LWCA operation are set up; these are:

- (1) Scan converter in RHI mode,
- (2) LWCA TO DISPLAY READ indicator forced ON
- (3) LWCA TO DISPLAY WRITE indicator forced ON if the converter memory buss is available (all STORE VIDEO switches OFF).

The scan converter ERASE VIDEO buttons used in normal operation do not erase the entire screen; the contour threshold legend area is left unchanged. In addition, a mask obscures from view certain areas within the ancillary data portion of the screen. These areas contain coded information available to the analyzer and needed by the contouring hardware. The ERASE DISPLAY buttons on the LWCA CONTROL PANEL not only erase the entire display, but also inhibit the mask so that the entire screen is available to display information from the processor. The mask and the legend are restored when the operator actuates the corresponding STORE THRESHOLDS button on the scan conversion processor.

The cursor can be made to appear in any display by depressing the appropriate CURSOR ON/OFF switch; the on state is indicated by illumination of the switch. The cursor, a blinking single point on the display, can be located anywhere on the screen by means of the CURSOR POSITION trackball.<sup>1</sup> The cursor changes color as a function of its surroundings so as to remain visible. During normal scan converter operation, the mask will obscure the cursor. If the cursor cannot be found, the following property may be useful: along the Top and Left edges of the display, the cursor will stop even if the trackball is rotated too far. At the bottom edge, the cursor disappears. When moved beyond the right edge, it reappears at the left where it finally stops about an inch from that edge; however, if the SEND DATA button were pressed with the cursor in such a position, the address would be wrong.

The color/intensity code covered by the cursor, as well as its coordinates, can be entered into the analyzer by pushing the appropriate SEND DATA button. The corresponding cursor must be switched-on for this action to be recognized. The SEND DATA switch will light when depressed, if the DDI control logic is in the proper state, and will extinguish about one-half second after the resulting interrupt has been serviced by the analyzer.<sup>1</sup> Pressing the INI button on the analyzer console should always turn off any SEND DATA indicators which are lit for whatever reason.

#### Display Conventions

The four display channels, numbered one through four, contain independent memories. Each memory is organized so that its address corresponds with the (X, Y) coordinates within a 248 by 320 point matrix as indicated in Figure 2. Each point can take on one of sixteen color/intensity combinations as listed in that figure. (The observed colors are a function of the settings of an array of switches in each memory interface unit; those colors listed correspond to the settings indicated in Figure 4-11 of Ref. 2.) Note that color 15 has a non-over write property: once this code occupies a point, the only way the color code at that point can be changed is by erasure.

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<sup>1</sup>. If any SEND DATA indicator is lit, no cursor will respond to the trackball.

The ancillary data area has significance only in normal scan converter operation; its outline is indicated in Figure 2, while the details of its contents appear in Figure 3. Information necessary for interpretation of the radar video data portion of the display (scaling, origin location, time, contour thresholds, and antenna angle) is obtainable by reading the four-bit codes in the patches indicated. Each of these patches contains the same four-bit code at all addresses within it. Most of the code patches have dimensions of 5 x 4 points (the same as the color patches) except for the origin location and scaling codes which are only 5 x 1. In either case, it is only necessary to read one point per patch, unless some sort of error correcting scheme is implemented to make use of the redundancy.

Points written as color 15 by a normally operating scan converter (not through the display data port) within the ancillary data area do not have the non-overwrite property. Any address in the ancillary data area which is not occupied by a 4 x 5 patch or an 8 x 5 character can be used for storage of a 4-bit word (e. g., to "mark" a stored video image) except for the 8 x 5 area under each color patch. Only the characters and color patches are displayed; everything else in the ancillary data area is masked. Again, the entire display area is erased (changed to color zero) and the mask is inhibited when an ERASE DISPLAY button is pushed, the entire area is now available to accept data from the analyzer.

#### General Comments on the Display Data Port

The hardware which comprises the display data port controller consists of two parts: an Interdata Universal Logic Interface (ULI) and a Raytheon-designed Display Data Interface (DDI). The ULI responds to device address X'8B' and contains interrupt and byte/halfword logic controlled by bits 0, 1 and 2 of the command byte (see Figure 4, note 2). Bit 2 should always be zero since the display data port operates only in the byte mode. Bits 0 and 1 affect interrupts in the following way: 01-interrupts enabled; 10-interrupts disabled but queued; 11-interrupts disarmed (neither accepted nor queued); 00-previous interrupt state unchanged. The ULI does not affect any bits in the status byte.

The DDI contains control logic which is described by the state diagram in Figure 4. Much of the notation here will not be of concern to the programmer. It is sufficient to note that state transitions are typically caused by execution of the 7/32 I/O instruction listed before the comment under each transition, or by a hardware-generated interrupt. Operation of the DDI control logic depends on the state of bits 4, 5 and 6 of the command byte as tabulated at the lower right of Figure 4. Also located there is a definition of the status byte, of which bits 3 through 7 are used.

### Write Display Memory

Three distinct types of write operations which might be useful in various situations are supported in the DDI control logic. Controlled by bits 4, 5 and 6 of the command byte (Figure 4), they include:

- (1) 0 0 0 - Write single point or multiple points the same color. The first write instruction transfers  $S_A$ ,  $X_{AM}$  and color code, while succeeding pairs of instructions transfer  $(X_A, Y_A)$ . The notation used here is explained in Figure 2; and the relationship to the Interdata bit numbers can be determined from Table 2.<sup>2</sup> This type of transfer might be useful where many points of the same color are to be plotted and it is not convenient to re-write  $S_A$ ,  $X_{AM}$  and the color code for each point. An example is listed in Table 2. After the initial write instruction, the following pairs correspond to halfwords so that a halfword table containing  $(X_A, Y_A)$  values could be easily accessed sequentially using a write block instruction.
- (2) 0 0 1 - Write single point or multiple points different colors. This sequence operates as the one described above, except that after the  $Y_A$  transfer, the next instruction transfers another number for  $S_A$ ,  $X_{AM}$  and color.
- (3) 0 1 0 - Write multiple points, fullword boundaries. This sequence operates as the one described above, except that after the  $Y_A$  transfer, the next instruction transfers nothing (see Figure 4, state W4), while the one following it transfers another number for  $S_A$ ,  $X_{AM}$ , and color. This type of operation is intended for sequentially writing from fullword tables where each fullword contains  $S_A$ ,  $X_{AM}$ , COLOR,  $X_A$  and  $Y_A$  for one point.

The Scan Converter, although it has an independent memory for each display, shares a memory address buss among the four display channels. When one or more STORE VIDEO switches is on, this buss is not available to the display data port and the write display memory operation is disabled in the hardware. It is also disabled for certain other switch settings as indicated in Table 1. Whenever the write operation is disabled, status bit 5 is zero. Before a write operation, it is good practice to check status to determine that bit 5 is one, although nothing will happen if a write is attempted, because the operation is disabled in the hardware. Status bit 4 should be checked to make sure it is zero; this bit indicates that a cursor data transfer is in progress and that the display data port is not available.

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<sup>2</sup>. See page 13 for table.

### Read Display Memory

There are two types of read operations, depending on whether or not the scan converter memory buss is available. If the buss is available (all STORE VIDEO switches off; status bit 7 = 1), then a normal read, which operates in much the same way as the write display memory transfer described in the preceding section, can be executed. Otherwise, the process must be a slow read, which involves an interrupt service routine. Both types of read operations are inhibited if the read indicator is not lit (status bit 6 = 0, see Table 1).

#### Read Display Memory -- Normal

An example of this type of data transfer appears in Table 2. First, the status is sensed to ensure that the memory buss is available, the read indicator is on, and that no cursor data entry is in progress. Next, the proper command byte is output to device X'8B' and SA, XAM, XA and YA are transferred just as for the write operation. At this point, a delay of at least six  $\mu$ sec; (for example, four BTCT 0, 0 (0200) instructions) must be executed so that the hardware is sure to have the required data ready. Lesser delays might work but have not been tried. Next, a read instruction is executed; the 4-bit color code appears in the four least significant bits of the second operand. Finally, a command byte can be output to leave the control logic in state I.

#### Read Display Memory -- Slow

If, in the preceding section, status bit 7 had been found to be zero, then a slow-read operation must be used. An example is found in Table 2. Steps 0 through 6 are the same as for a normal read, except that interrupts are enabled. The control logic, after step 6, ends up in state SR4 (see Figure 4) where it waits for an interrupt. This wait could last as long as 16 milliseconds and ends when the DDI has obtained data. Other processing can be executed during this wait interval. When the interrupt occurs, a simple interrupt service routine consisting of steps 8 through 10 of the example in Table 2 completes the operation.<sup>3</sup>

---

<sup>3</sup>. Details on interrupt processing can be found in Interdata Documents:

Model 7/32 Reference Manual, Pub. No. 29 - 399R02, Section 2.4  
32-Bit Series        "        "        Pub. No. 29 - 365R01, Chapter 7.

### Cursor Data Entry

As does the slow-read operation, the cursor data entry makes use of an interrupt service routine and a data acquisition method which does not require the scan converter memory buss. There is, however, no long delay because, following the pressing of a SEND DATA button, no interrupt is generated until after all required data has been obtained. The cursor data entry requires that the DDI control logic be in state I and that the ULI has interrupts enabled; hence, step 0 of the example in Table 2. The remainder of this example is an interrupt service routine which checks the status to see that the interrupt was caused by a cursor data entry, outputs a command byte to disarm further interrupts, then transfers  $S_C$ ,  $X_{CM}$ ,  $X_C$  and  $Y_C$  to the second operand locations of the three read instructions. Finally, the control logic is returned to state I, interrupts are again enabled, and the original program status word is restored.

### Programming Examples

The SCPLT subroutine listed in Table 3 was used in the Liquid Water Content display subroutine to take care of getting the ninth bit of X in the right place and to execute the necessary IO instructions for writing one point. The inputs were left in registers and the subroutine was called using BAL F, SCPLT. Because no other data transfer modes were being used in this application, the command byte was programmed to always leave the ULI with interrupts disarmed. SCPLT is called many times during the main program; it always leaves the control logic in state I. But in order to ensure that the very first point is plotted, the following instructions should be executed before SCPLT is called for the first time:

```
LHI    B, X'8B'  
OC     B, DDICMD2
```

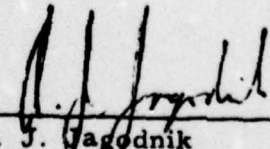
Thus forcing the control logic to state I.

Another way to structure SCPLT would put what is now line 72 (Table 3) after line 58, thus SCPLT would not leave the control logic in state I, but would force it there first each time it is called. A third method would involve forcing the control logic to state I only once, then not using any OC instructions at all in SCPLT itself. This method is the simplest and fastest, but depends on nothing disturbing the control logic between calls of SCPLT, where it would be left in state RW1 (Figure 4).

Table 4 lists a program to copy one display to another. It was written directly in machine language as a diagnostic to test the hardware, which it does very well since it accesses all display memory locations and exercises the read circuitry in the source display and the write circuitry in the output display. A good test of the hardware would consist of the following:

- 1) Store a test pattern or radar data image which contains all 16 colors in display 1; erase displays 2, 3 and 4.
- 2) Put Q = 0 0 0 0 and P = 0 0 2 0 into the program and run. Displays 1 and 2 should now be identical.
- 3) Put Q = 0 0 2 0 and P = 0 0 4 0 into the program and run. Displays 1, 2 and 3 should now be identical.
- 4) Put Q = 0 0 4 0 and P = 0 0 6 0 into the program and run. All displays should be identical.
- 5) Erase display 1.
- 6) Put Q = 0 0 6 0 and P = 0 0 0 0 into the program and run. All displays should again be identical.

Table 4 is shown set up for a normal read; to exercise the slow read, follow the directions at the end of the table. Execution of the copy program takes about three seconds in the normal read mode, and five seconds in the slow read mode. If the full 16 milliseconds delay were incurred at every point in the slow read mode, the program would require over 21 minutes for execution. The reason it only takes 5 seconds lies in the format adopted for scanning in the copy program. Examination of Table 4 will reveal that the copy process is basically accomplished by reading one point from the source display, writing that data into the same address in the output display, incrementing by one to the next Y address, then repeating. When Y reaches 248, X is incremented by one and Y goes back to zero. The fact that Y changes more rapidly than X is the key to the reason for the unexpectedly fast performance in the slow read mode. The average delay is only about 67 microseconds because of the way in which the copy-program scan interacts with the display raster-scan.

  
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C-9

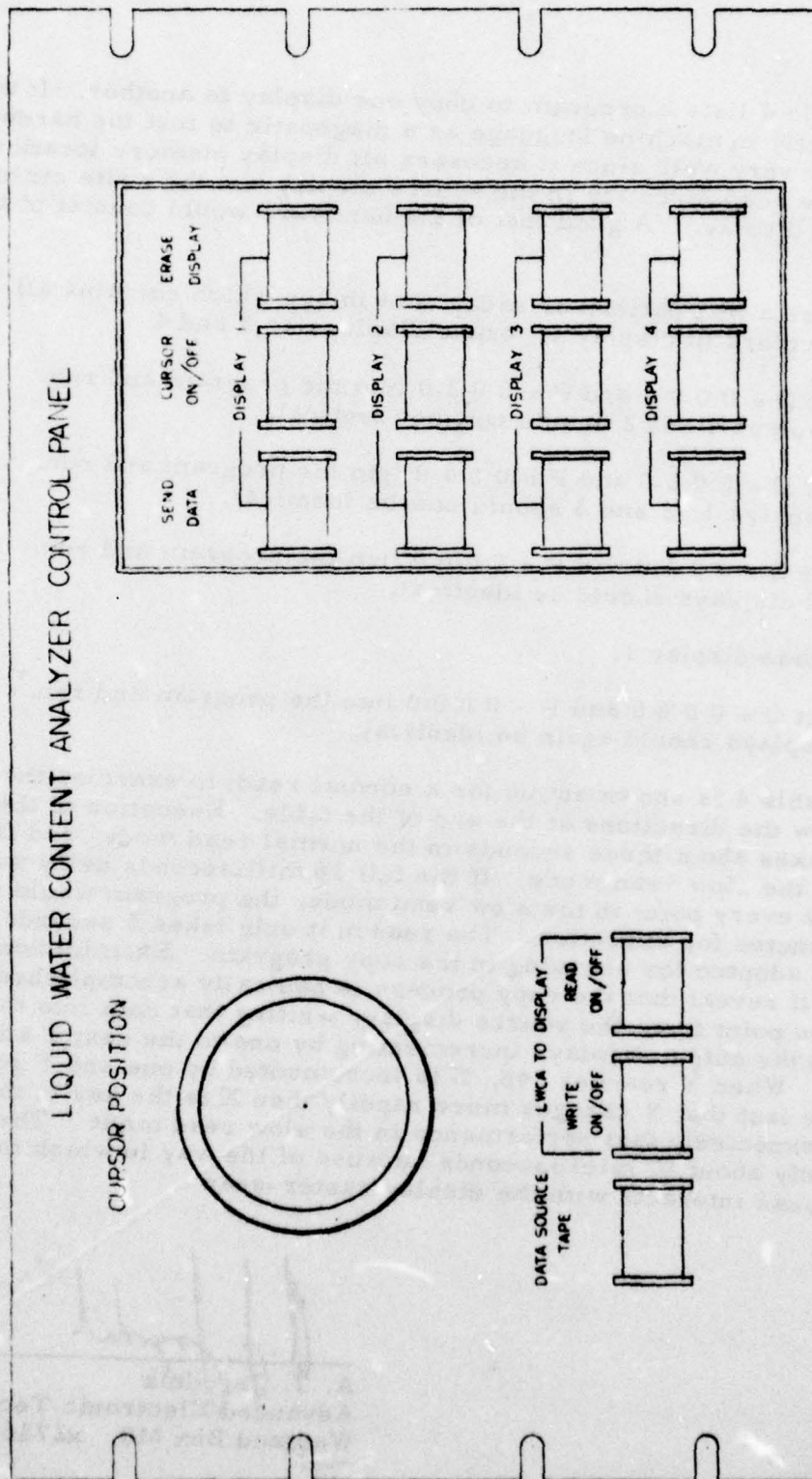


Figure 1. Control Panel

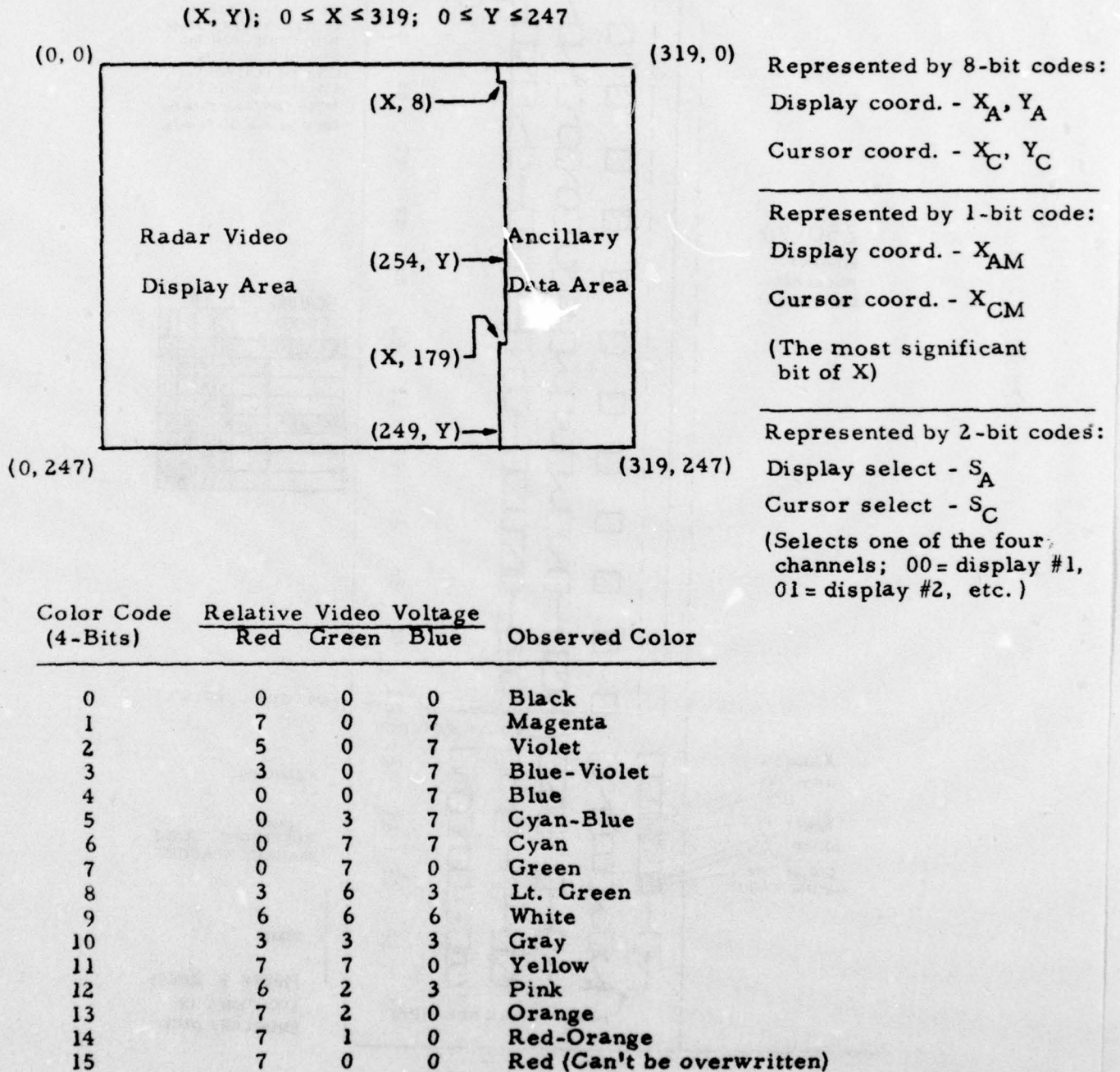


Figure 2. Display Addressing and Color Code Conventions for Each of the Four Channels

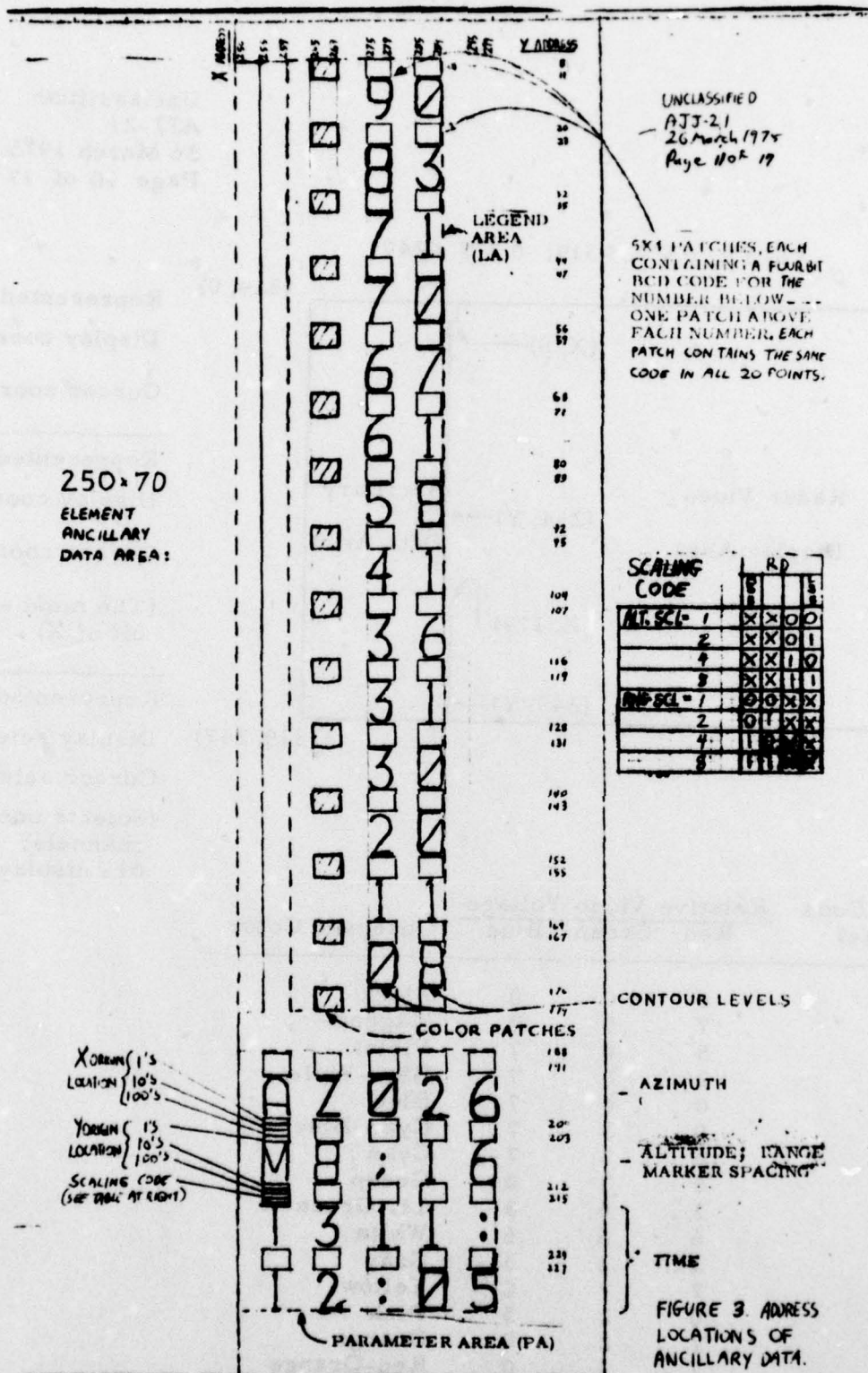




TABLE 2  
 EXAMPLES OF DISPLAY DATA PORT I/O OPERATIONS (FOR INTERRUPT DRIVEN I/O: I/O TABLE LOC. X'E16-X'D0'42 (284 HZ: X'80'))  
 MUST CONTAIN THE ADDR OF THE INT. SERV ROUTINE

OPERATION	TYPICAL STEPS	VLS INPUTS			VLS OUTPUTS			VLS TIME	VLS TYPE	VLS CONTROL LOGIC
		DIN (DATA)	SIN (STATUS)	INT (INTERRUPT)	DOT (DATA)	COT (CONTROL)	INT (INTERRUPT)			
WRITE DISPLAY MEMORY (TWO RUNS THE SAME COLOR)	0. SENSE STATUS	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0
	1. CHECK STATUS FOR OKX									
	2. OUTPUT (NO BYTE OR INT)									
	3. OUTPUT (NO BYTE)									
	4. TRANSFER SA, XA, AND COLOR DATA									
	5. TRANSFER FIRST XA									
	6. TRANSFER FIRST YA									
	7. TRANSFER SECOND XA									
	8. TRANSFER SECOND YA									
READ DISPLAY MEMORY (NORMAL MODE ALLOWED I/O SINCE IT IS TRUE DURING THE SLOW READ MUST BE USED IN NEXT PAGE)	0. SENSE STATUS	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0
	1. CHECK STATUS FOR OKX									
	2. OUTPUT (NO BYTE OR INT)									
	3. OUTPUT (NO BYTE)									
	4. TRANSFER SA, XA									
	5. TRANSFER XA									
	6. TRANSFER YA									
	7. DELAY - 64 SEC									
	8. TRANSFER COLOR DATA									
CURSOR DATA ENTRY (INTERLU- SCHEDULE R. TIME)	0. OUTPUT (NO BYTE)									
	1. OBSERVE PULSE ON SA TN LINE (MAYBE INTERRUPT)									
	2. CHECK STATUS, IN REGS, FOR BIT 19 THE NLE, ETC									
	3. OUTPUT (NO BYTE, DATA INTERRUPT)									
	4. TRANSFER SC, XC, AND COLOR DATA									
	5. TRANSFER XC									
	6. TRANSFER YC									
	7. OUTPUT (NO BYTE, INTERRUPT)									
	8. RESTORE PAGE STATUS, WORD									

0. INT AVAILABLE AT VLS OUTPUT  
 1. INT NOT AVAILABLE AT VLS OUTPUT

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# DISPLAY DATA PORT I/O OPERATIONS (CONT.)

OPERATION	TYPICAL STEPS	TYPICAL MESSAGE INSTRUCTIONS	VLI INPUTS		VLI OUTPUTS		VLI CLOCK TIME MS	TYP TIME MS
			DIN (ms)	SIN (ms)	DOUT (ms)	COT (ms)		
READ DISPLAY MEMORY (SLOW)	0. SENSE STATUS	SS	0. . . . . 0	0. . . . . 0	0. . . . . 0	0. . . . . 0	0	0
	1. CHECK STATUS FOR OXIO							
	2. OUTPUT END BYTE IN LMS	OC						
INTERLUPT SENSE ROUTINE	3. OUTPUT END BYTE, ENABLE INTERRUPT	OC						
	4. TRANSFER SA, XA	WD						
	5. XA	WD						
	6. TA	WD						
	7. INTERRUPT WHEN DATA IS READY (DOUT WILL WAIT BETWEEN 0 AND 16 MICROSECONDS)	—						
	8. TRANSFER COMA DATA RD	RD						
	9. OUTPUT END BYTE	OC						
	10. RESTORE PROG STATUS WORD	LDWR						

② DISPLAY  
 CURSOR  
 SELECT  
 CODES

S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	DISC <sub>0</sub>
0	0	0	0	1
0	1	0	1	2
1	0	1	0	3
1	1	1	1	4

TABLE 3. SCPLT Subroutine

00000821	C8B0	003B		58	SCPLT	LHI	B,X'8B'	Device code in reg. B.
00000861	DEB0	4000	00BE1	59		OC	B,DDICMD1	Output Cmd-disarm int, DDI to st. RW1.
000008C1	C900	0100		60		CHI	X,X'100'	Compare X to 256.
00000901	4210	4000	00B01	61		BM	SCPLTA	If X < 256, go to SCPLTA.
00000961	C800	0100		62		SHI	X,X'100'	Decrease X by 256.
000009A1	CAC0	0010		63		AHI	C,X'10'	Make bit 27 of C a 1.
000009E1	9AEC			64		WDR	B,C	Write cont of reg C (SA,XAM,Color).
00000A01	9AED			65		WDR	B,X	" " " " X (input X-256).
00000A21	CAD0	0100		66		AHI	X,X'100'	Restore X to what it was.
00000A61	CBC0	0010		67		SHI	C,X'10'	" C " " " "
00000AA1	4300	4000	00B41	68		B	SCPLTB	Go to SCPLTB.
00000B01	9AEC			69	SCPLTA	WDR	B,C	Write cont of reg C
00000B21	9AED			70		WDR	B,X	" " " " X
00000B41	9ABE			71	SCPLTB	WDR	B,Y	" " " " Y
00000B61	DEB0	4000	00C01	72		OC	B,DDICMD2	Output Cmd-disarm int,DDI to st. I.
00000B81	030F			73		BR	F	Return to the address in reg. F.
00000BE1				74		ALIGN	2	
00000C01	C200			75	DDICMD1	OC	X'C200'	
00000C01	CE00			76	DDICMD2	OC	X'CE00'	

INPUTS: Reg. X, x-coord.  $0 \leq X \leq 319$   
 Reg. Y, y-coord.  $0 \leq Y \leq 247$   
 Reg. C, S in bits 25&26, color in bits 28-31,  
 all other bits zero.  
 Reg. F, return address.

TABLE 4. Program to copy one display to another.

6000	C8A0	LHI	A,Q	source display: 1 2 3 4
2				Q ; 0000 0020 0040 0060
4	C8B0	LHI	B,P	output display: 1 2 3 4
6				P : 0000 0020 0040 0060
8	C880	LHI	8,8B	device code in reg. 8.
A	008B			
C	C890	LHI	9,C8	cmd byte for read in reg. 9.
E	00C8			
6010	C850	LHI	5,C2	cmd byte for write in reg. 5.
2	00C2			
4	24D0	LIS	D,0	zero reg. D.
6	24E0	LIS	E,0	" " E.
8	9E89	OCR	8,9	output cmd byte for read.
A	9A8A	WDR	8,A	write S <sub>A</sub> ,X <sub>AM</sub>
C	9A8D	WDR	8,D	" X <sub>A</sub>
E	9A8E	WDR	8,E	" Y <sub>A</sub>
6020	0200	BTCH	0,0	delay (No-op)
2	0200	BTCH	0,0	"
4	0200	BTCH	0,0	"
6	0200	BTCH	0,0	"
8	9B8C	RDR	8,C	read data into reg. C.
A	C4C0	NHI	C,F	mask all but the 4 lsb of reg. C.
C	000F			
E	9E85	OCR	8,5	output cmd byte for write.
6030	0ACE	AR	C,B	get the output display code in reg. C.
2	9A8C	WDR	8,C	write S <sub>A</sub> ,X <sub>AM</sub> ,Color
4	9A8D	WDR	8,D	" X <sub>A</sub>
6	9A8E	WDR	8,E	" Y <sub>A</sub>
8	26E1	ALS	E,1	increment Y <sub>A</sub> by 1.
A	C9E0	CHI	E,F8	compare Y <sub>A</sub> with 248
C	00F8			
E	4320	BNP	6018	if Y <sub>A</sub> ≤ 248, go to 6018.
6040	4000			
2	6018			
4	26D1	ALS	D,1	increment X <sub>A</sub> by 1.
6	24E0	LIS	E,0	zero Y <sub>A</sub> .
8	C9D0	CHI	D,100	compare X <sub>A</sub> with 256.
A	0100			
C	4210	BN	6018	if X <sub>A</sub> < 256, go to 6018.
E	4000			
6050	6018			
2	4330	BNE	6064	if X <sub>A</sub> ≠ 256, go to 6064.
4	4000			
6	6064			
8	C9D0	CHI	D,13F	compare X <sub>A</sub> with 319.
A	013F			
C	4320	BNP	6018	if X <sub>A</sub> ≤ 319, go to 6018.
E	4000			
6060	6018			

(continued)

TABLE 4 (Continued)

6062	2200	BFBS	0,0	branch unc. to self.
4	CAAO	AHI	A,10	add 16 to reg. A (make $X_{AM}=1$ ).
6	0010			
8	CABO	AHI	B,10	" " " " B " "
A	0010			
C	4300	B	6018	go to 6018.
E	4000			
6070	6018			

To do the same task using the slow read mode, change:

600E	004A			cmd byte for slow read, interrupts enabled.
6020	2200	BFBS	0,0	branch unc. to self.

and include the following interrupt service routine:

6100	2612	AIS	1,2	increment reg. 1, the loc part of the PSW, by one halfword to bypass the 2200 at 6020.
6102	1800	LPSWR	0,0	restore the PSW

Run with immediate interrupts enabled, in reg. set 0. (PSW=4000)  
 In the interrupt service pointer table, at  $DO+2x8B$ , put the  
 starting address of the interrupt service routine:

0E16	6100
------	------

Note: This program was written directly in machine language; it was never assembled by CAL. The assembler notation included here is incorrect for CAL in that all numbers listed are in hex. In CAL, such numbers must be represented as X'NNNN' or F'NNNNNNNN', except for 0-9.



FORM 10-0557 (9-65) BOND

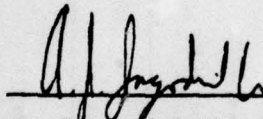
DIVISION EQUIPMENT  
Operation EDL  
Department ADL - Wayland

To File  
From A. J. Jagodnik, Jr.  
Subject SCRM Drawing List

Classification	Unclassified
Contract No.	-
Distribution	cc
File No.	-
Memo No.	AJJ-49
Date	26 July 1976

Reference: AJJ-26 memo dated 4 June 1976.

The fact that three different SCRM (Scan Converter Refresh Memory) systems have been built and extensively modified in different ways has led to some confusion in the area of the applicability of drawings. The Table contained herein is intended to resolve the confusion. It contains all drawings related to the scan converters, ordered by Raytheon drawing number, and indicates the equipment to which each is applicable. Also included is information describing the size, type and form of each drawing master and whether or not it references other drawings.

  
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SCRM DRAWINGS

Page 1 of 3

[S - Schematic, I - Interconnection Diagram, M - Mechanical,  
B - Block Diag.]

[V - Vellum, M - Mylar, S - Sepia]

Dwg No.	Size	Type	Form	Abbrev. Title (Notes)	Application					
					SCRM 2 Before		KMR		SCRM 3	
					LWCA	KMR	LWCA(2)	Master	Remote	Master Remote
895180	B	M	V	Mtg. Brkt. Interface	(MIU Shelf)	X	X	X	X	X
895181	D	S	V	C.C. X Hatch Gen	3C	X	X	X	X	X
895182	D	S	V	Test Card		X	X	X	X	X
895183	D	S	V	C.C. Origin Trans. BCD/BW	3F	X	X	X	X	X
895184	D	S	V	C.C. X Proj. Accum	3E	X	X	X	X	X
895185	D	S	S	C.C. Hi Alt Acc	2C	X	X	X	X	X
895186	D	S	S	C.C. Lo Alt Acc	2D	X	X	X	X	X
SD895187	D	S	S	AIU	3D	X	X	X	X	X
895188	D	S	V	C.C. Y Proj. Accum		X	X	X	X	X
895189	D	M	V	Hole Layout, Rear Pnl Interface #1 (Lower SCP)		X	X	X	X	X
895190	D	M	V	" " " " #2 (Upper SCP)		X	X	X	X	X
895191	D	M	V	" " " " #3 (MIU)		X	X	X	X	X
895192	D	S	S	C.C. T. F. Earth Alt. Acc.	2E	X	X	X	X	X
895193	D	S	S	C.C. R. Proj. Accum	2F	X	X	X	X	X
SD895194	D	S	V	VDU		X	X	X	X	X
895195	D	S	S	C.C. Alt 12 x 12 Mult.	1F	X	X	X	X	X
895196	D	S	V	C.C. Range 12 x 12 Mult.	1E	X	X	X	X	X
895197	E	B	V	C.C. Block Diag.		X	X	X	X	X
895198	E	S	V	C.C. X 12 x 12 Mult.	1A & B	X	X	X	X	X
895199	E	S	S	C.C. Y 12 x 12 Mult.	1C & D	X	X	X	X	X
SD895200	E	S	S	MIU (2 sht)		X	X	X	X	(1)
SD895201	E	S	1-V	DCU (2 sht)		X	X	X	X	(1)
895202	E	S	S	C.C. Alt Compar.	2A & B	X	X	X	X	X
895203	E	S	V	C.C. Interface	3A, B & C	X	X	X	X	X
895204	E	M	S	S.C. Front Panel, Hole Layout		X	X	X	X	X
895205	E	M	V	S.C. Silk Screen Layout		X	X	X	X	X
895718	J	I	S	Int. Diag-KMR CC*		X	X	X	X	X
895720	E	S	S	KMR Master SCRM F & R Panels*		X	X	X	X	X
895726	C	I	S	KMR Master SCRM Power Supplies		X	X	X	X	X
897392	E	I	V	C.C. Interconnect*		X	X	X	X	X
897393	C	I	1-V	Scan Conv. Interconnect*		X	X	X	X	X
897896	B	I	S	MEM to MIU (Cable)		X	X	X	X	X
897897	C	I	V	DCU & VDU to MIU (Cables)		X	X	X	X	X
897898	E	S	V	S.C. Proc. F & R Panels*		X	X	X	X	X
897899	E	I	V	DCU to VDU*		X	X	X	X	X
897900	C	I	V	S. C. Proc. DC Power Supplies		X	X	X	X	X

SCRM DRAWINGS (Continued)

Page 2 of 3

Dwg No.	Size	Type	Form	Abbrev. Title (Notes)	Application											
					SCRM 2		SCRM 1		(2)		KMR		SCRM 3			
					Before	LWCA	KMR	Before	LWCA	KMR	Master	Remote	Master	Remote		
897918	B	S	V	Term for Twp Lines												
910161	D	M	V	Hole Layout F Panel												
910162	D	M	S	Silk Screen F Panel												
910163	C	M	V	Bracket for Conn.												
910166	D	S	V	LWCA Control Panel												
910167	C	I	V	Cable: LWCA Control or Disp. Int. Panel to DDI												
910168	E	S	S	DCU (2 sht)												
910169	J	S	S	MIU (Sections C-F; G. Dennis has mylar from which this was made)*												
910170	C	S	V	Mon. No. 5 input sel.				X								
910171	E	S	V	Color Encoder (MIU Same as SD895200 sht 2)								X				
910172	C	I	V	Cable - DCU to Card 2											X	
910173	D	I	S	Cable - DDI to ULH											X	
910174	D	I	V	Cable - DDI to DCU												
910175	E	S	M	DDI												
910176	D	I	V	LWCA Scan Conv. *												
911046	C	S	V	Data Trans Control Panel & Cable												
911047	D	S	M	SDF												
911048	E	S	M	DRU												
911049	D	I	M	Remote Refresh Memory *											X	
911050	D	I	V	Cables - KMR Master*											X	
911101	C	I	S	KMR Master SCRM*											X	
911102	E	S	S	KMR DCU (Sht 2 same as SD895201 sht 2)											X	
911103	E	I	S	KMR DCU to VDU*											X	
911104	J	S	S	Master KMR MIU (C-F; G. Dennis has mylar from which this was made)*											X	
911155	B	I	V	Remote MIU Video Jumper											X	
911156	D	I	V	RRM F & R Panels											X	
911157	D	M	V	Silk Screen - F. Panel Data Trans. Ctrl.											X	
911158	D	M	V	Silk Screen RRM												
911159	D	M	S	Hole Ly F Panel RRM												
911160	D	M	S	Hole Ly F Panel Data Trans Ctrl											X	

Dwg. No.	Size	Type	Form	Abbrev. Title (Notes)	Application	
					Master	Remote
SD913301	B	S	V	Power Control Panel	X	
SD913302	C	I	V	Aux. Video J12, 13, 14 to VDU	X	
913303	C	M	V	Modem Front Panel Layout & Silk Screen	X	X
SD913304	C	S	V	Data Transmission Control	X	
913305	C	I	V	Cables SDF/VDU to Modem & Infoton		X
913306	C	I	V	Cables DRU to Modem and Infoton		X
913307	D	M	V	Silk Screen & Hole Ly Remote Ref. Mem. Rcvr.		
913308	D	M	V	Silk Screen & Hole Ly Data Transmission Control	X	
913309	D	M	S	Silk Screen Layout Display Interface Panel	X	
913310	D	M	S	Hole Layout Display Interface Panel	X	
SD913311	D	S	S	SDF/VDU, Section E	X	
SD913312	D	S	S	SDF/VDU, A, B & C*	X	
SD913313	D	S	S	SDF/VDU, Section F	X	
SD913314	D	S	S	SDF/VDU, Section D	X	
913315	D	I	V	Cables SDF to DDI (3 cables)	X	
913316	E	M	S	Silk Screen Front Panel (SCP)	X	
913317	E	I	S	Interconnection Diagram DCU & VDU	X	
913318	E	M	S	Hole Layout Front Panel (SCP)	X	
913319	E	S	S	SCP Front & Rear Panel (Wiring)	X	
SD913320	E	S	S	C.C. X 12 x 12 Mult.	X	
SD913321	E	S	S	C.C. Interface	X	
SD913322	E	S	S	DRU		X
SD913323	E	S	S	DDI	X	
SD913324	E	S	S	DCU (2 sheets)	X	
913905	D	S	S	Display Interface Control Panel	X	
SD914328	D	I	S	Cables DDI to DCU & MAG. (5 Cables)	X	
SD914329	D	I	S	SCRM 3 Master*	X	
SD914330	C	I	V	Cable SDF - MAG.	X	
SD914331	C	S	V	SDF/VDU, Section C*	X	
SD914332	E	S	S	Color Encoder (MIU)	X	
SD914333	D	S	M	MAG	X	
SD914334	J	S	S	Master MIU*	X	
914358	D	M	S	Hole Ly Rear Panel, Interface #1	X	
914711	D	I	S	Remote Refresh Memory - SCRM 3*		X

\* Other Drawings Referenced

(1) See 911049, Note 2.

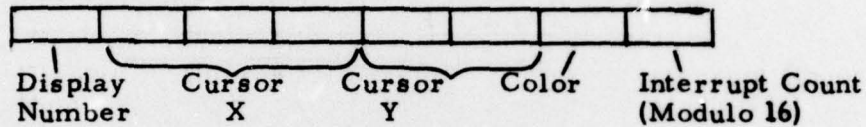
(2) All LWCA drawings are not listed here; only those related to the SCRM.

## APPENDIX D

### SOFTWARE FOR TESTING HARDWARE

(See also Table 4 of AJJ-21, Appendix C)

# DDI CURSOR DATA ENTRY TEST PROGRAM DISPLAY AS FOLLOWS



<u>Location</u>	<u>Value</u>			
2 0 0 0	C 8 6 0	LHI	R6, X'DD'	
2	0 0 D D			
4	C 8 8 0	LHI	R8, X'8B'	Device Code for ULI
6	0 0 8 B			
8	C 8 9 0	LHI	R9, X'4E'	Cursor ARM
A	0 0 4 E			
C	9 E 8 9	OCR	R8, R9	ARM Cursor Interrupt
E	2 4 5 0	LIS	R5, 0	Initialize Interrupt Counter
1 0	2 2 0 0	B	*	Hang
2 0 2 0	9 E 8 6	OCR	R8, R6	Setup ULI for Read
2	2 6 5 1	AIS	R5, 1	Increment Interrupt Count
4	0 2 0 0	NOP		
6	9 B 8 A	RDR	R8, R10	Input Display, XMSB, Color
8	9 B 8 B	RDR	R8, R11	Input X
A	9 B 8 C	RDR	R8, R12	Input Y
C	9 E 8 9	OCR	R8, R9	Reset Interrupt
E	C 8 7 0	LHI	R7, X'40'	Incremental Code
3 0	0 0 4 0			
2	2 4 4 1	LIS	R4, 1	Display Panel (Hex) Device Code
4	9 E 4 7	OCR	R4, R7	Setup Hex Display
6	0 8 7 A	LR	R7, RA	First Word
8	1 0 7 4	SRLS	R7, 4	Position Display and X-MSB

# DDI CURSOR DATA ENTRY TEST PROGRAM (Continued)

<u>Location</u>	<u>Value</u>			
2 0 3 A	0 4 7 4	NR	R7, R4	X-MSB Only
C	9 4 B B	EXBR	R11, R11	Exchange X Bytes
E	0 6 B 7	OR	R11, R7	Add in X-MSB
4 0	0 8 7 A	LR	R7, RA	First Word Again
2	1 0 7 1	SRLS	R7, 1	Position Display Number
4	C 4 7 0	NHI	R7, X'30'	Display Bits Only
6	0 0 3 0			
8	C A 7 0	AHI	R7, X'10'	Make Number 1-4
A	0 0 1 0			
C	0 6 B 7	OR	R11, R7	Add to X Value
E	C 4 A 0	NHI	R10, X'F'	Color Only
5 0	0 0 0 F			
2	0 8 7 5	LR	R7, R5	Counter
4	C 4 7 0	NHI	R7, X'F'	Keep Modulo 16
6	0 0 0 F			
8	1 1 A 4	SLLS	R10, 4	Position Color
A	0 6 7 A	OR	R7, R10	Now have color and Counter
C	9 4 7 7	EXBR	R7, R7	Exchange bytes for output
E	0 6 C 7	OR	R12, R7	Add to Y Value
6 0	9 8 4 C	WHR	R4, R12	Output Y, Color, Counter
2	9 8 4 B	WHR	R4, R11	Output Display, X
4	1 8 0 0	LPSWR	0	Exit Interrupt
0 1 E 6	2 0 2 0	DC	X'2020'	Interrupt Trap Address

Run Program from X'2000' after insuring that the  
PSW is X'4000'.

If Not X'4000', perform following:

```
INI DATA X'4000' FN 1
DATA X'2000' ADD INI RUN
```